DDR200/266 Memory Bus Design & Evaluation

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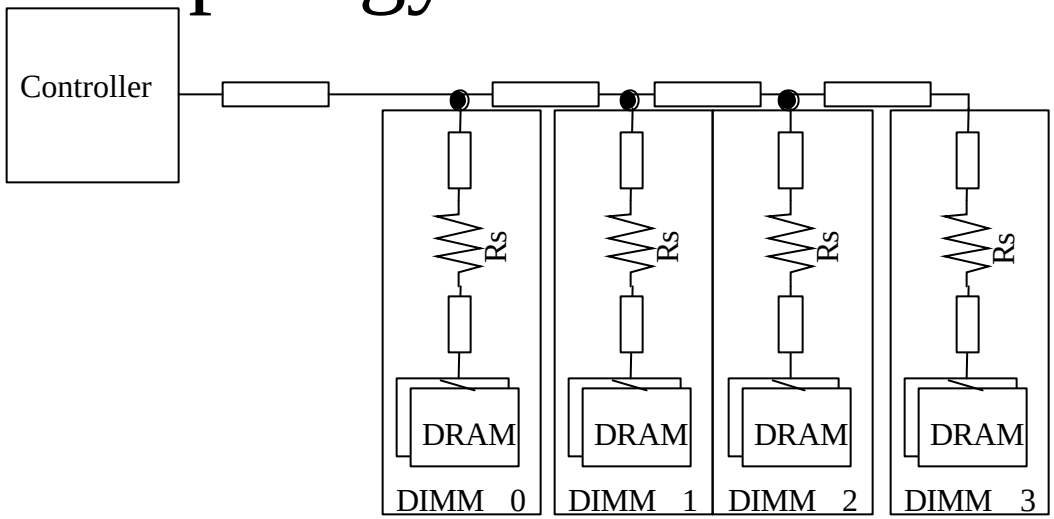
Problems with High speed

- CLK Rate Increase -> Timing Margin Decrease
  - Setup/Hold Margin
  - Jitter/Skew Margin
  - Inter Symbol Interference
- Edge Rate Increase -> Signal Integrity Loss
  - Cross Talk
  - Reflection
  - Simultaneous Switching Noise
- Swing Level Decrease -> Noise Margin Decrease
  - Signal Integrity
  - Vref Noise

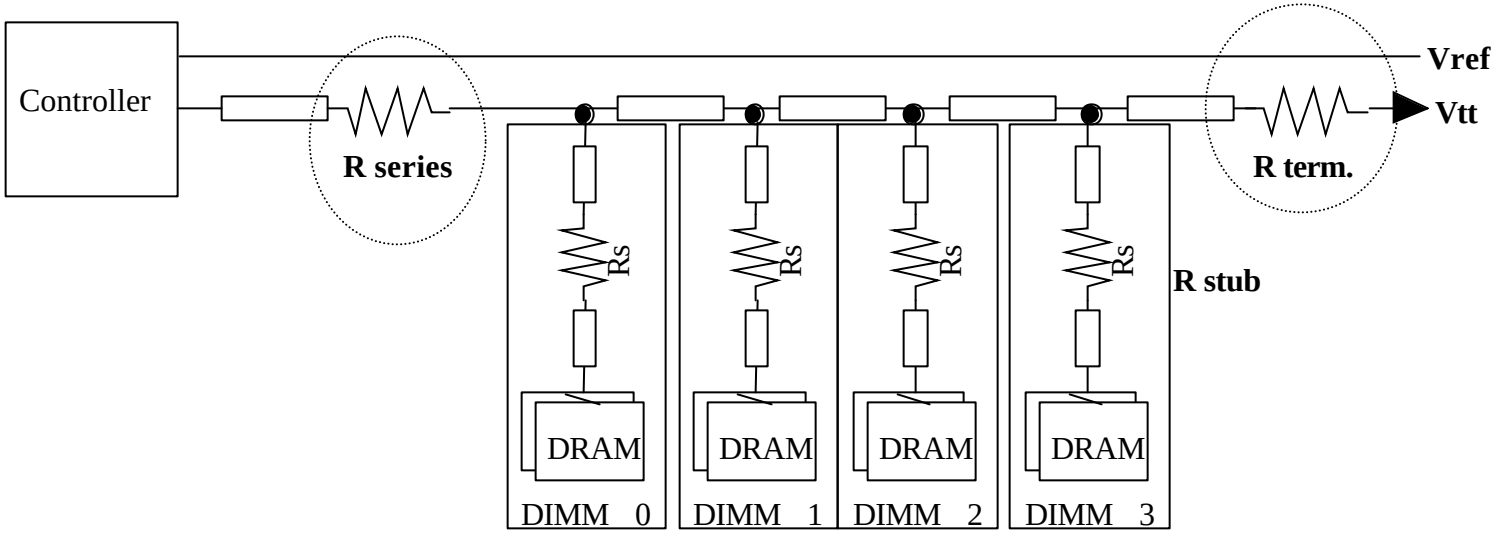
Difference between PC133 and PC266

	PC266	PC133
Address Rate	7.5ns	7.5ns
Command Rate	7.5ns	7.5ns
Data Rate	3.75ns	7.5ns
Interface	SSTL	LVTTL
Min Swing	700mV	1.2V
Data Clocking	Source(DQS)	Global(CLK)
tAC	+-700ps	5.4ns
tDS	500ps	1.5ns
tDH	500ps	0.8ns

Topology of LVTTL and SSTL2

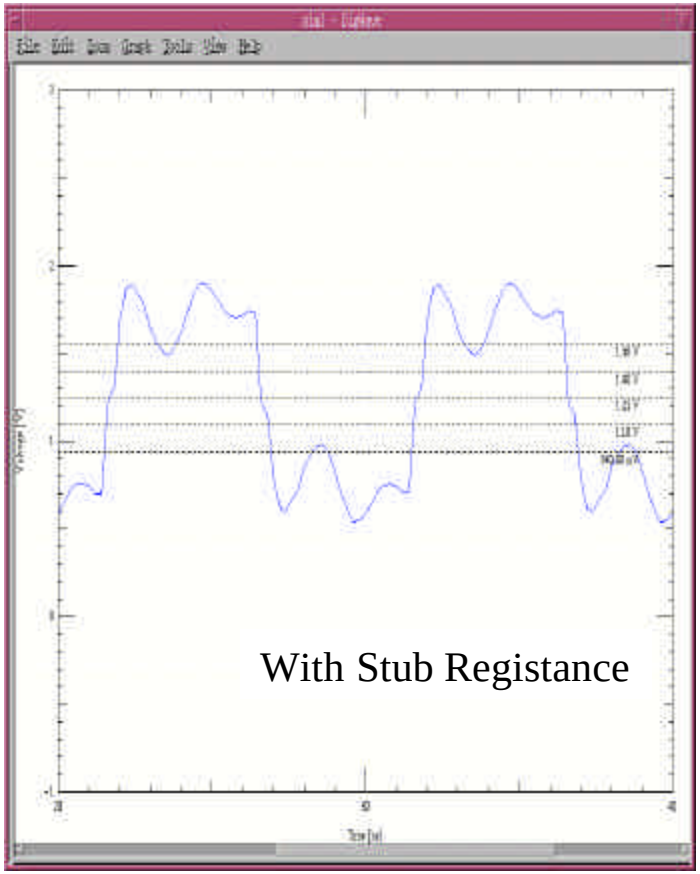


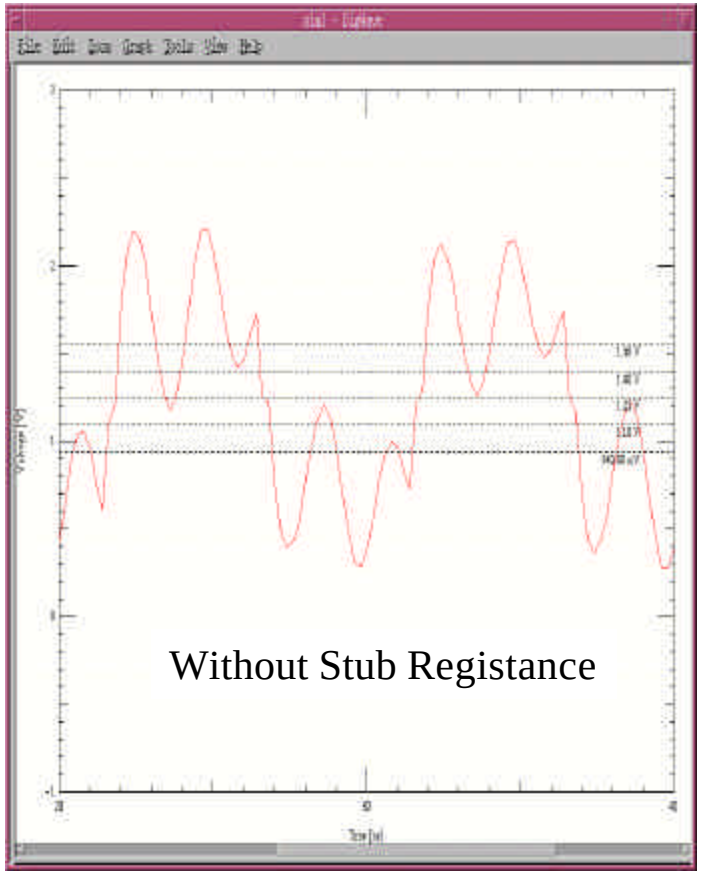
Conventional SDRAM memory bus topology (LVTTL)



DDR SDRAM memory bus topology (SSTL2)

Function of Stub Registance

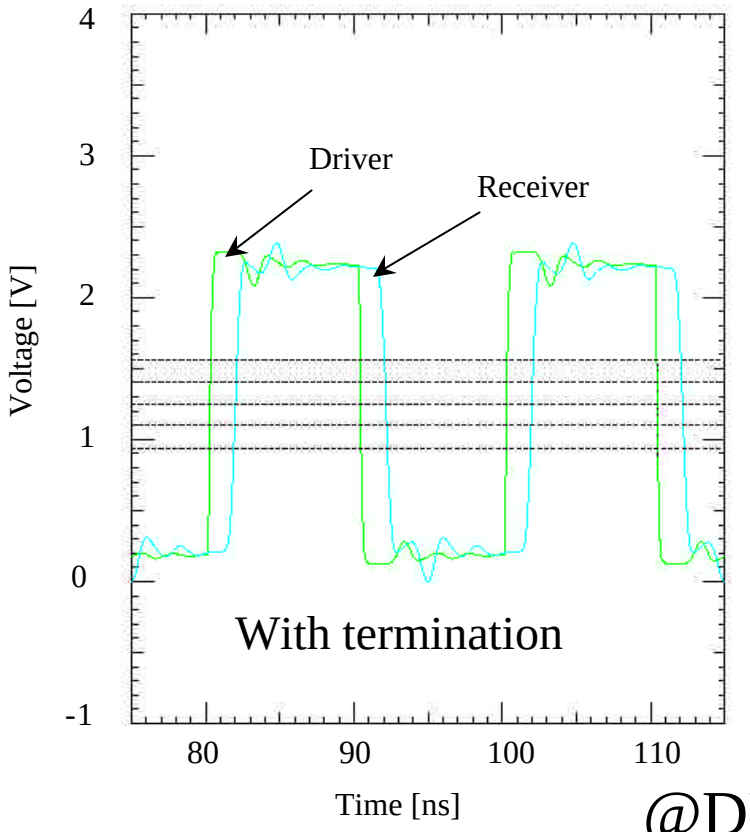


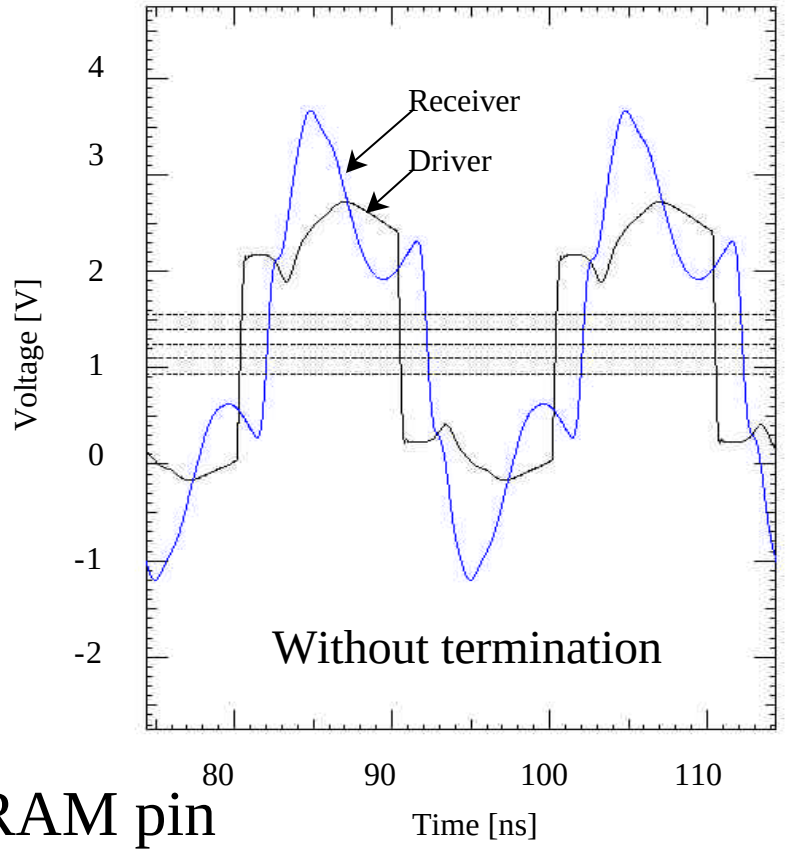


@DRAM pin

reduces reflection at the stub of transmission line

Function of Paralell Termination



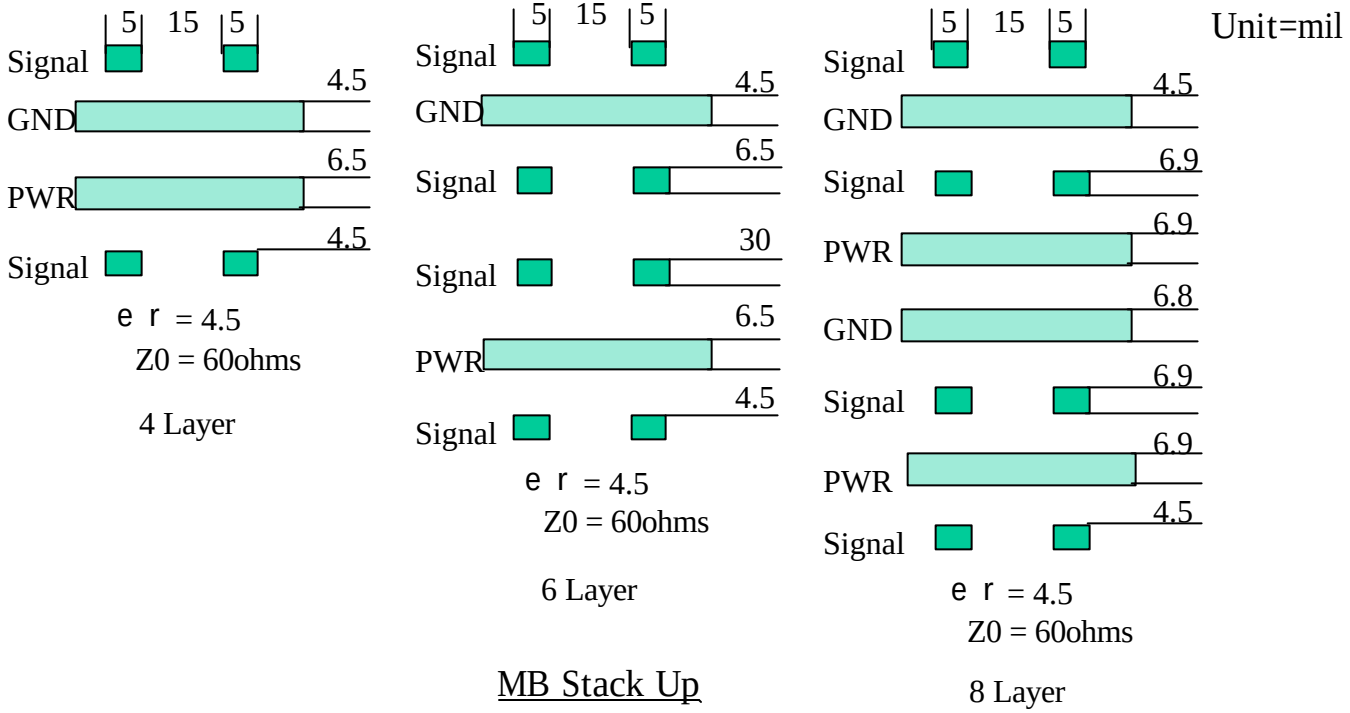


@DRAM pin

reduces reflection at the end of transmission line

PCB Layer Stackup

- Impedance
- Crosstalk

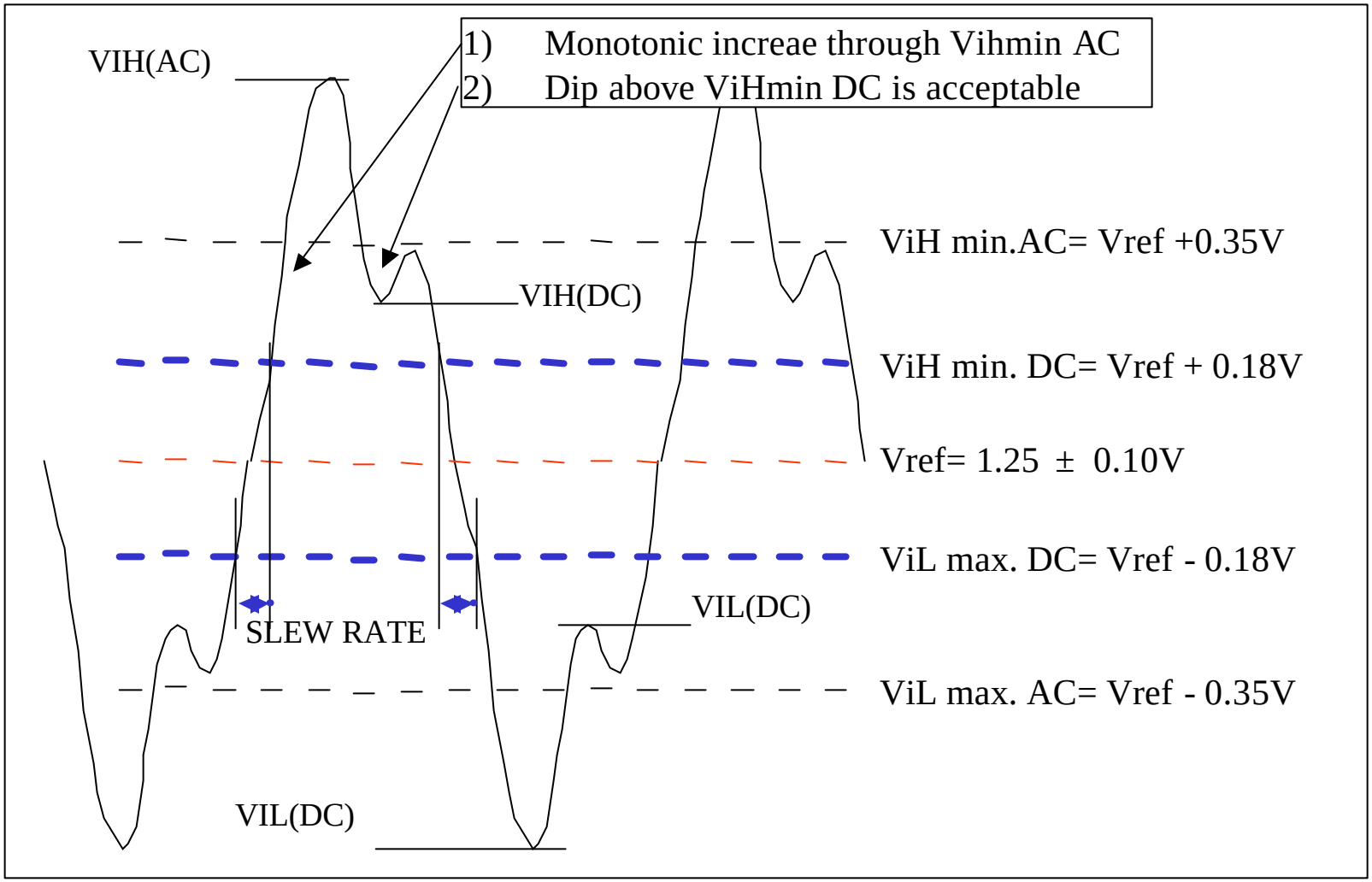


MB Stack Up

Simulation_Tools

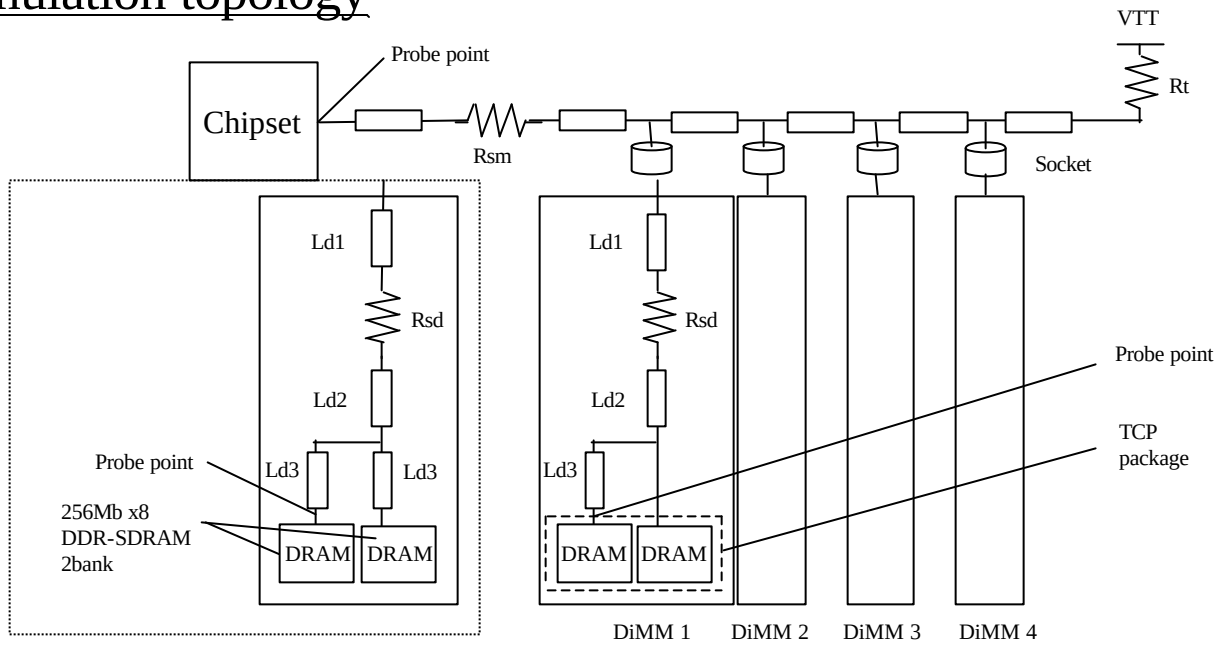
No.	Vendor	Tool	Task
1	Cadence	ConceptHDL	Circuit Diagram
2	Cadence	APD	PCB Layout
3	Cadence	SigNoise	Post-Layout Simulation
4	Applied Simulation Technology	Apsim RLGC	PCB Modeling
5	Ansoft	Signal Integrity, Maxwel	PCB Modeling
6	Avant!	HSPICE	Pre-Layout Simulation

Input Level Definitions



Pre Layout Simulation

Simulation topology



1GB (TCP)

Ld1= 3.7 (mm)

Ld2=25.2 (mm)

Ld3= 1.2 (mm)

(TSOP)

Ld1= 3.5 (mm)

Ld2=16.2 (mm)

Ld3= 9.5 (mm)

Fig.1 System topology (1GB TCP,TSOP)

Sensitivity test parameters

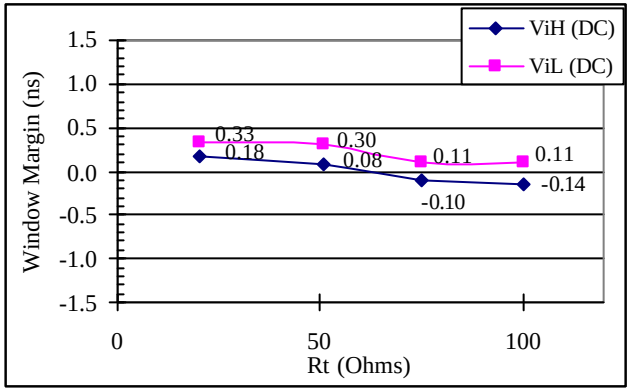
	symbol	Value			unit	Simulation	
		Min	Typ	Max		Heavy	Light
(1)	Rsm : Motherboard stab resistance	10	22	50	ohm	○	○
(2)	Rt : termination resistance	20	50	100	ohm	○	○
(3)	Rsd : DiMM stab resistance	10	22	50	ohm	○	○
(4)	Lss : socket pitch	5	11	20	mm	○	
(5)	Lcs : length between chipset and socket	50	65	100	mm	○	
(6)	Lst : length between socket and termination resistance	50	10	30	mm	○	

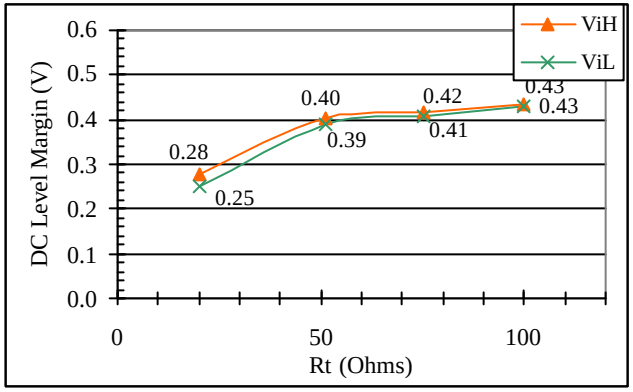
Typ : base condition

○ : Simulated

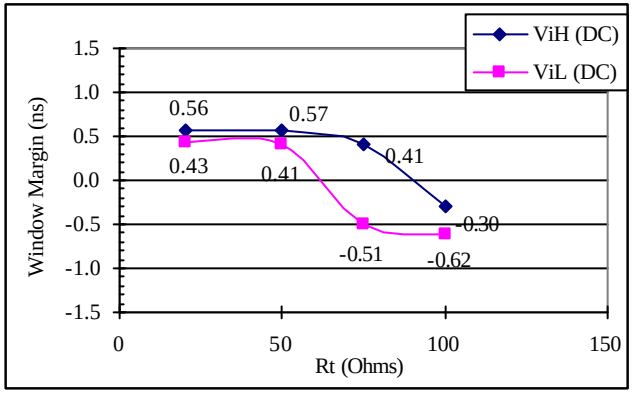
Sensitivity Test (termination resister dependency)

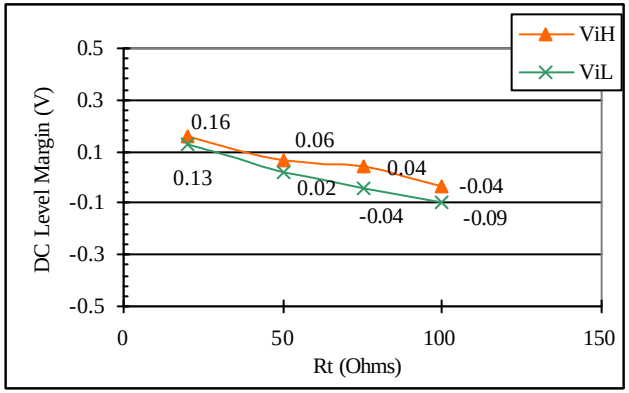
a) Write operation :Rt=20,51,75,100 (Ohms)



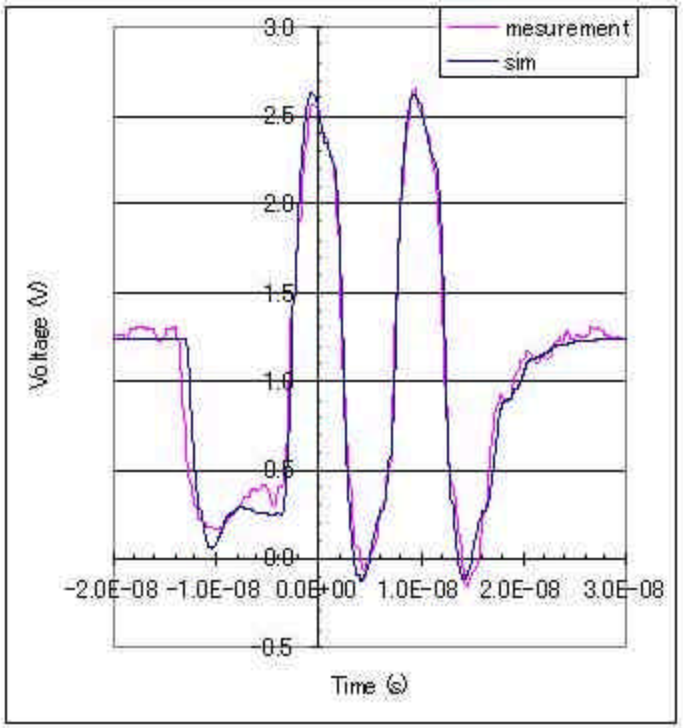


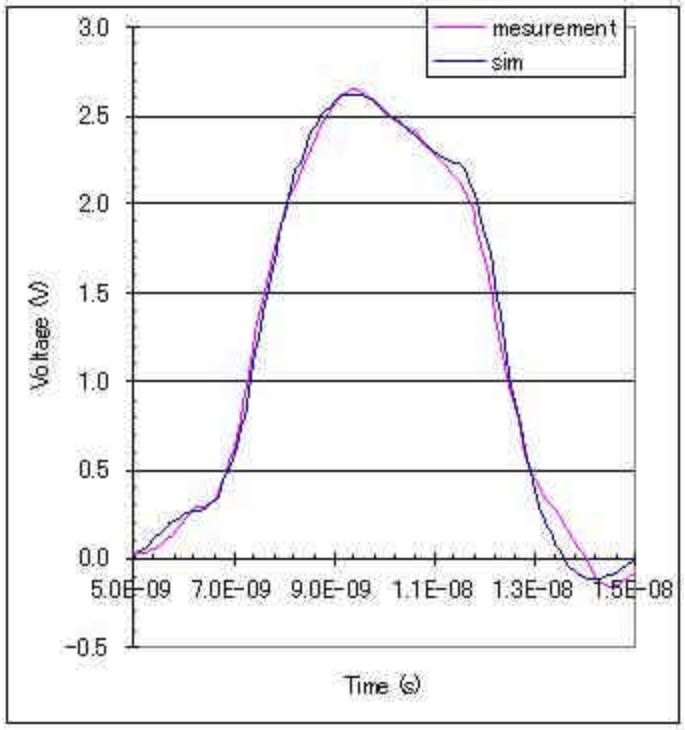
b) Read operation :Rt=20,51,75,100 (Ohms)





Measurement & Simulation correlation (1GB TCP module)

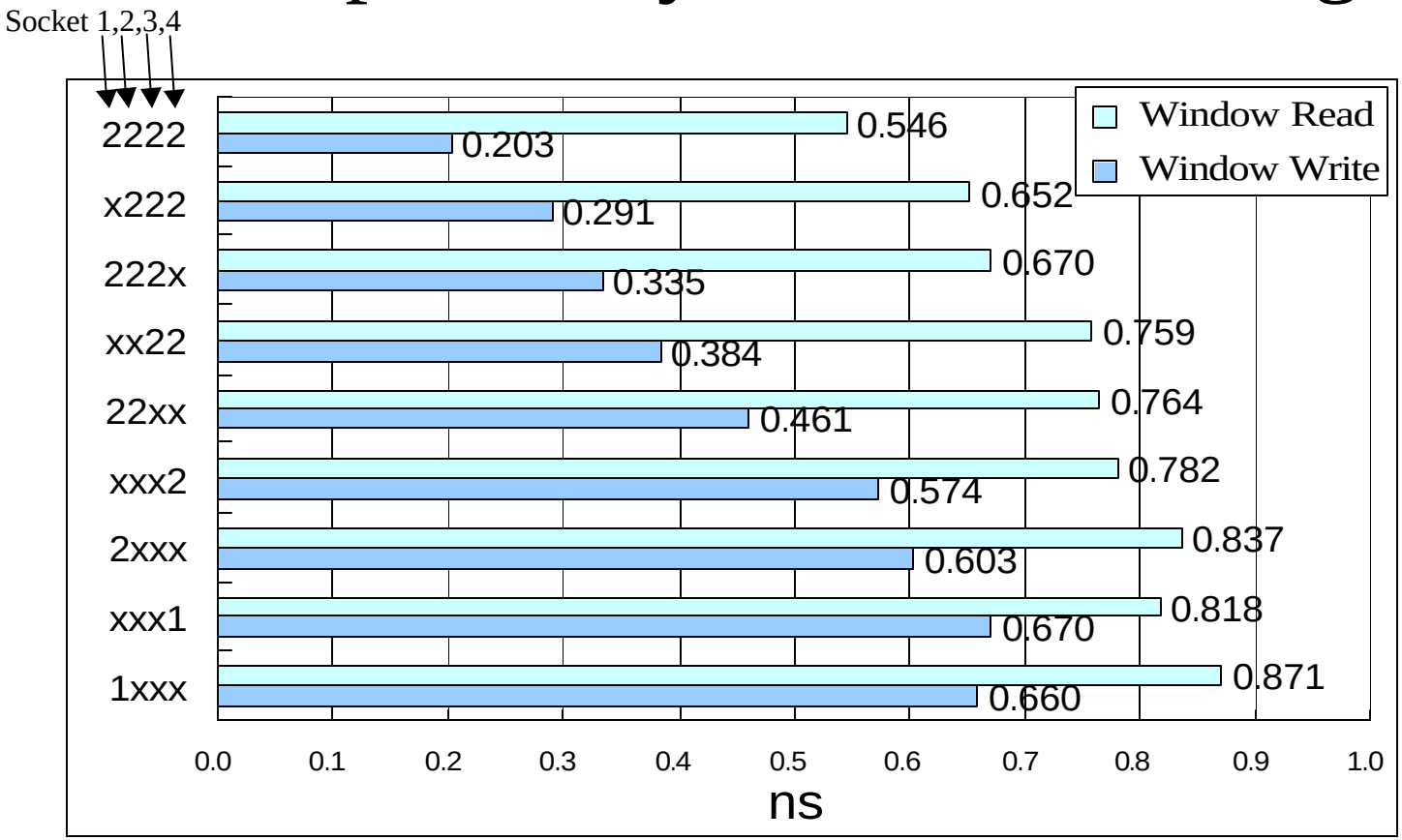




Partially enlarged figure

DQS signal measurement & simulation

Load dependancy of Window margin



Socket 1 is closest to controller.

The number indicates number of module banks. X indicates empty socket.

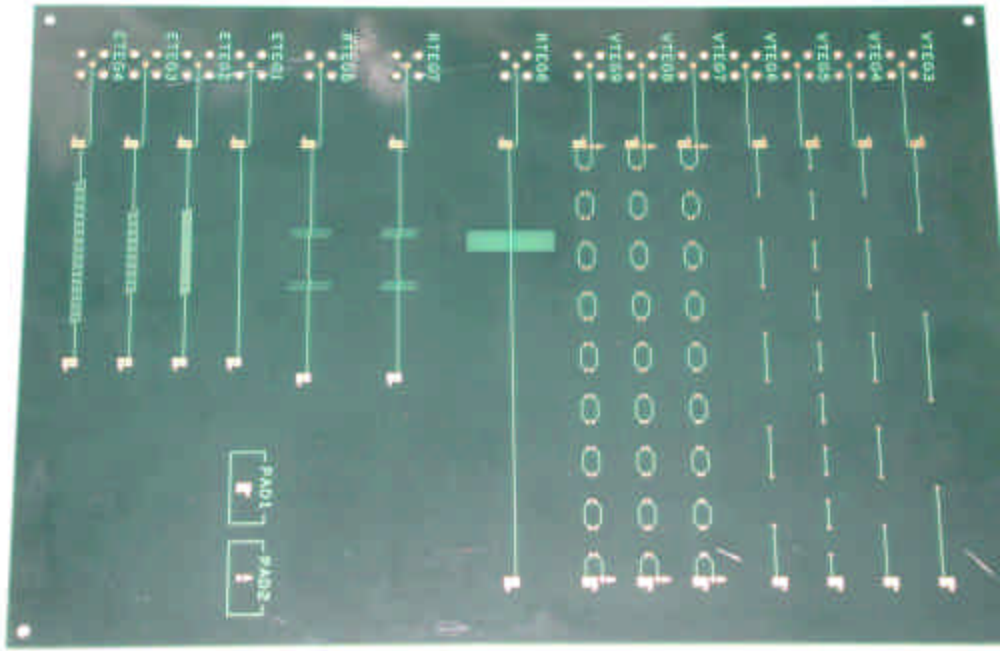
i.e. 22xx means 2 2 bank DiMMs in the sockets closest to controller and other slots empty.

Recommends to start populating sockets closest to paralell termination.

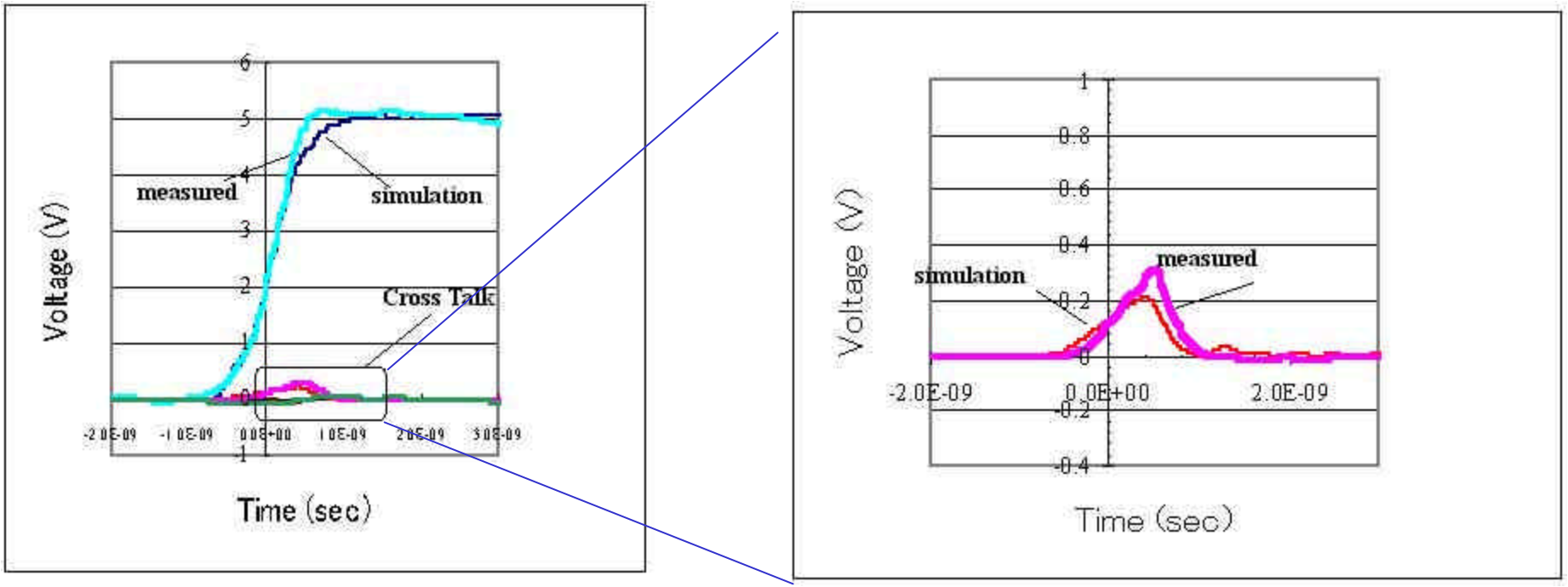
Further study of PCB simulation

Following design elements have been examined using TEG and Simulator

- Cross talk
- VIAs
- Transmission delay
- Return current



Results example (cross talk)



Partially enlarged figure

Cross talk TEG measurement & simulation

ELPIDA

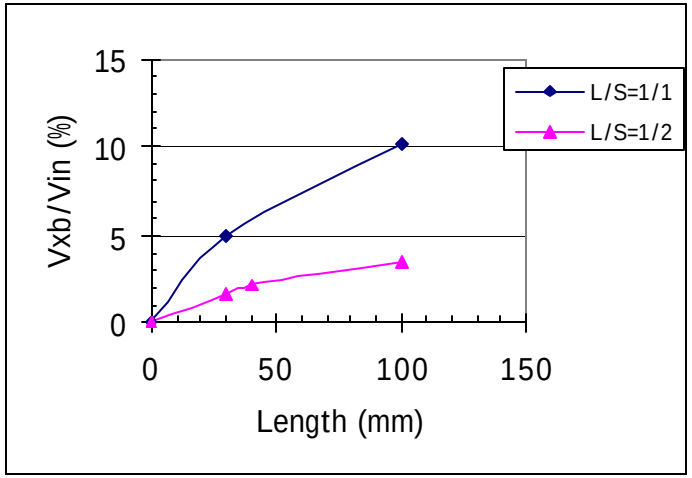
General Layout Considerations

Platform Conference

Routing space- cross talk

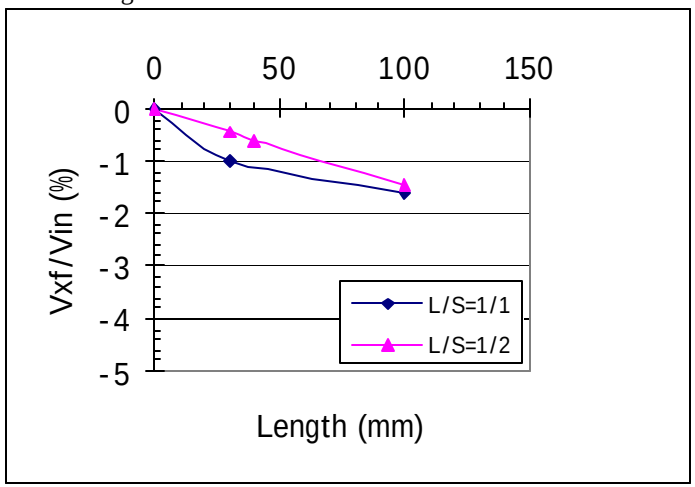
1. Length dependancy(backward)

*L/S=1/1=112u/118u L/S=1/2=112u/250u
Tr: 5.74ns/V Z0=59ohm



2. Length dependancy(forward)

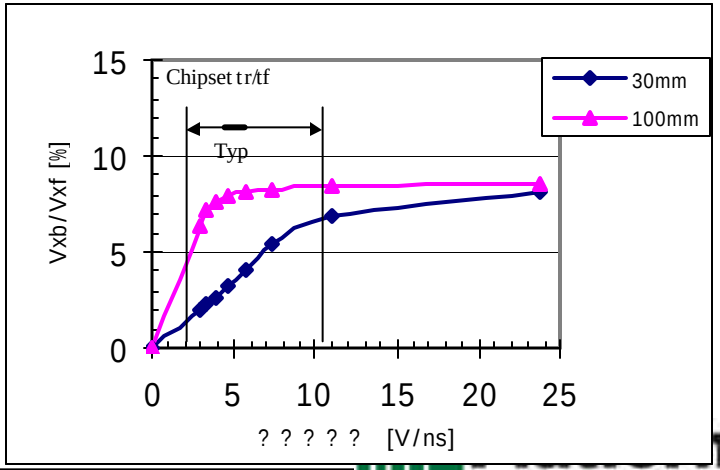
Wire length:100mm? Tr: 5.74ns/V



- For Kb<2.5%, length of parallel routing< 50mm@L/S=112/250um

3. Transient time dependancy(backward)

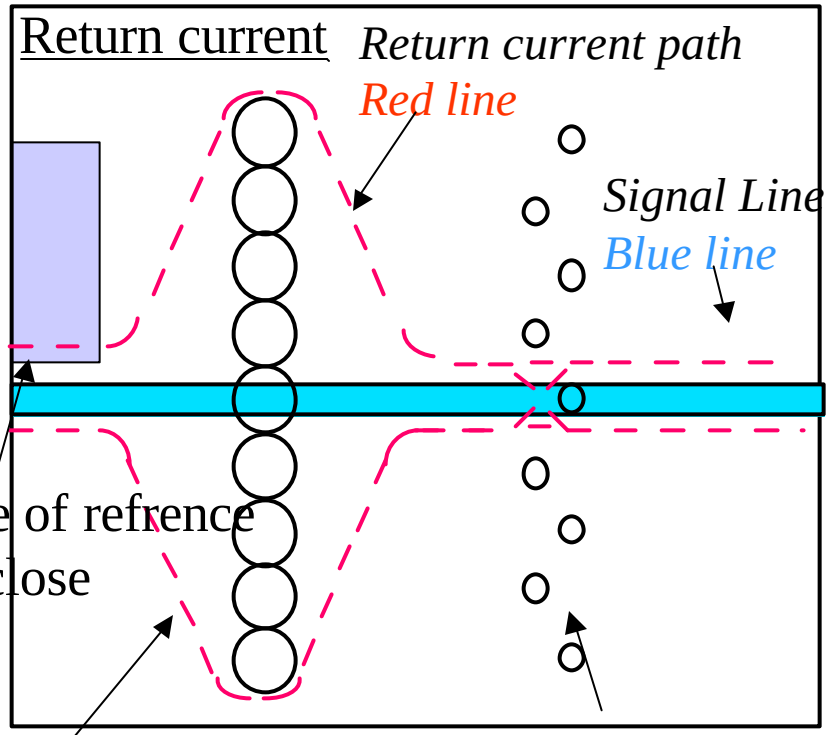
*L/S=1/1=112u/118u



Routing Space Recommendation(for 60ohm line):

- Signal travelling same direction :15mil.
- Signal travelling opposite direction :20mil.

VIA placement - return current,cross talk



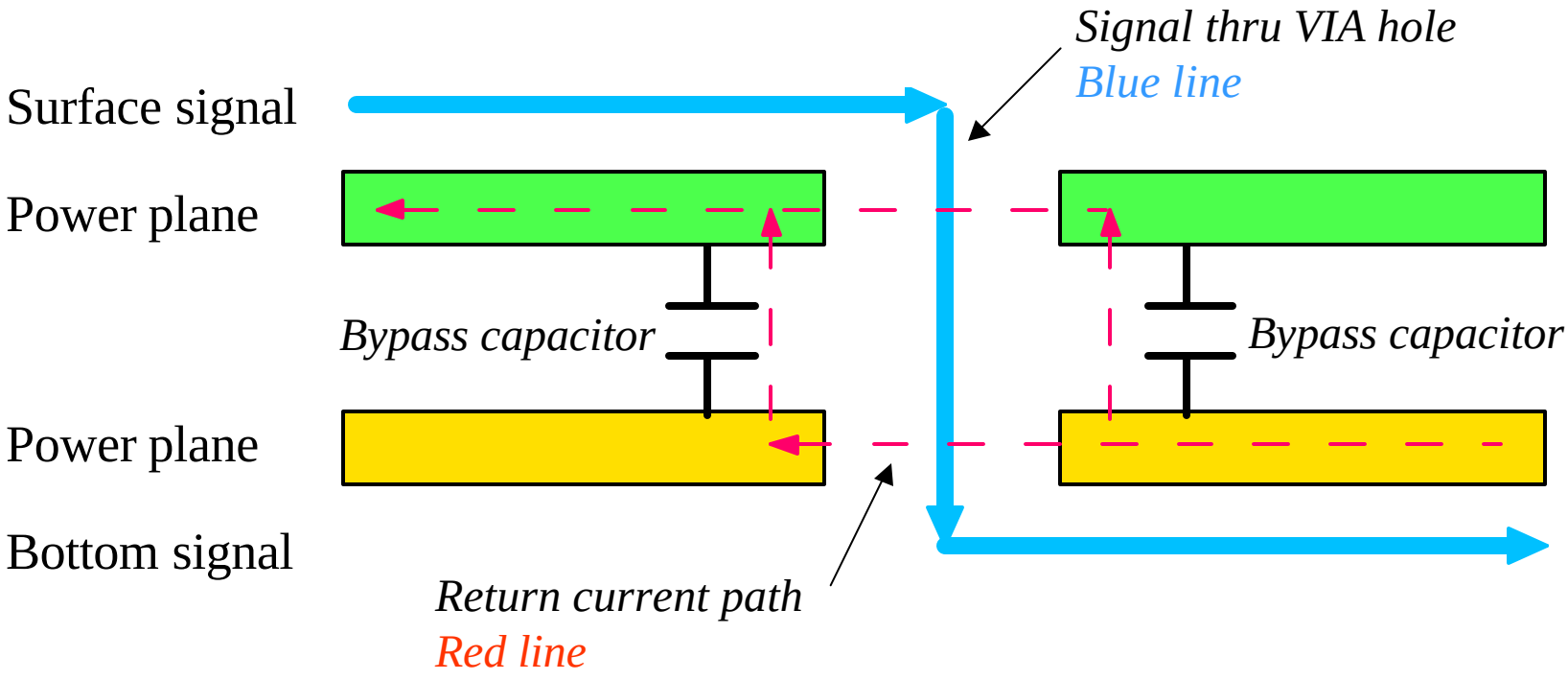
VIA-VIA Cross talk

VIA-VIA pitch	Cross talk coeficient
0.75mm	0.33 %/via
0.95mm	0.24 %/via
1.15mm	0.20 %/via
1.50mm	0.15 %/via

PCB thickness=1.24mm

Allow at least 0.2mm between anti-pads to provide return path.
Leave the thickness of dielectric between the edge of refrence plane & wire.
Allow at least 1.5mm between signal VIAs to reduce cross talk.

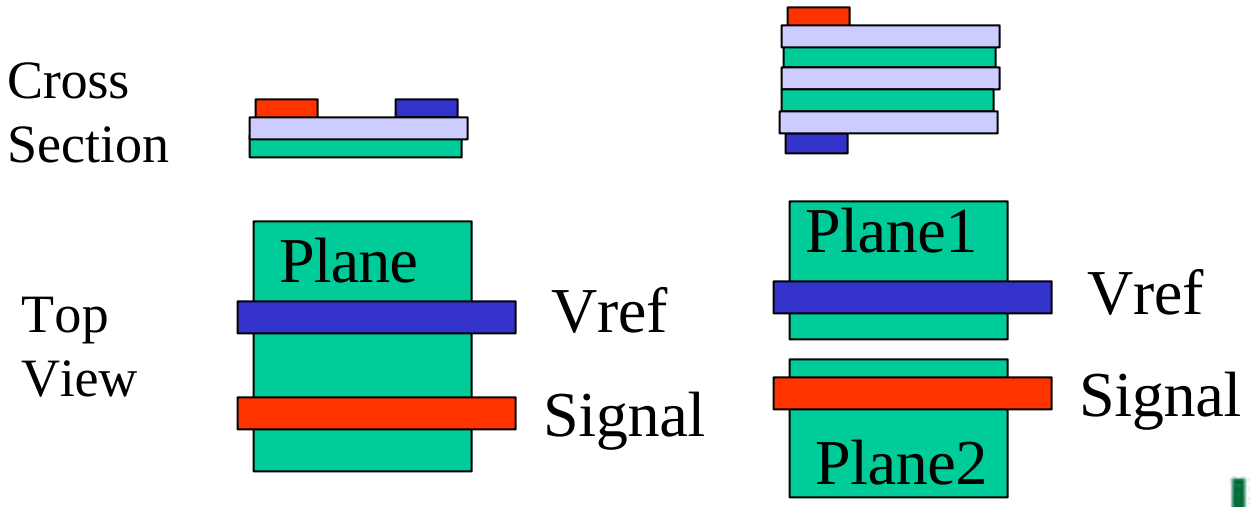
Bypass capacitor placement –return current



· Minimize layer change of high speed signal.
· When change layer, try to have a bypass capacitor to provide return path.

Vref

- Noise on Vref reduces timing margin.
  - SSTL uses differential inputs of Vref and signal.
  - Route Vref refrence to GND layer.
  - Leave more than 30mil from signal line to reduce cross talk.
  - Route Vref with more than 30mil trace to reduce impedance.
  - Have several pads for adjusting decoupling capacitor at the both end of Vref line.



Data Synchronization

- Source Synchronous BUS- preserve timing relationship with Data & Data strobe
  - Matched length & topologies required

  - Length : ball to pin : less than 1mm difference.
    microstrip line=6ps/mm, strip line=6.8ps/mm
  - Layer : surface is faster : use same layer
  - # of VIA : reduces impedance : use same # 0f VIA
  - # of turns : short turns are faster : use same radius of turns

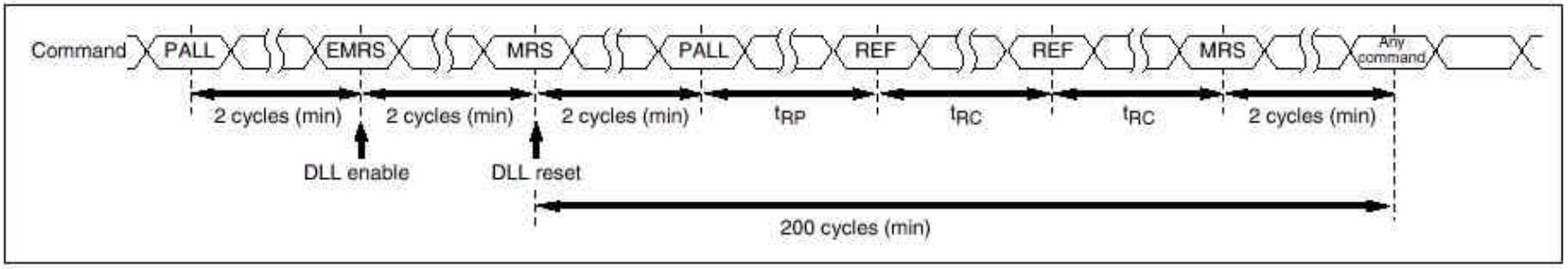
BIOS consideration

- Power up Sequence
- Buffer Strength
  - CMD,ADDR,DQM,DQS,DQ loading
  - 2 bank DiMM
  - Registered DiMM
- Refresh Rate
  - 256Mb requires 7.8us refresh rate
- Memory Timings
  - When using BL=1, tRAS min>45ns

Power-up Sequence(DDR Specification)

1) Apply power and maintain CKE at an LVCMOS low state (other inputs may be undefined).
   Apply VCC before or at the same time as VCCQ .
   Apply VCCQ before or at the same time as VTT and VREF .
2) Start clock and maintain stable condition for a minimum of 200 µs.
3) Issue NOP command and take CKE high.
4) Issue precharge all command for the initializing device.
5) Issue EMRS to enable DLL.
6) Issue a mode register set command (MRS) for "DLL reset" with bit A8 set to high
   (An additional 200cycles of clock input is required to lock the DLL after every DLL reset).
7) Issue precharge all command for the device.*1
8) Issue 2 or more auto-refresh commands.*1
9) Issue a mode register set command to initialize device operation.

Note: *1. Sequence of (7) and (8) may be reversed.



256MB R-DiMM

	Component Organization	DQ Loading	Refresh
9 pcs of 256Mb 1bank	x8	x1	7.8us
18 pcs of 128Mb 1 bank	x4	x1	15.6us
18 pcs of 128Mb 2banks	x8	x2	15.6us
36 pcs of 64Mb 2banks	x4	x2	15.6us

Same module capacity can be achieved with different components and requires different chip set setting.

Chipset DRAM Timing Register Setup(1)

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes utilized by module manufacturer	1	0	0	0	0	0	0	0	80	128
1	Total number of bytes in serial PD device	0	0	0	0	1	0	0	0	08	256 byte
2	Memory type	0	0	0	0	0	1	1	1	07	SDRAM DDR
3	Number of row address	0	0	0	0	1	1	0	1	0D	13
4	Number of column address	0	0	0	0	1	0	1	1	0B	11
5	Number of DIMM banks	0	0	0	0	0	0	1	0	02	2
6	Module data width	0	1	0	0	1	0	0	0	48	72 bit
7	Module data width continuation	0	0	0	0	0	0	0	0	00	0 (+)
8	Voltage interface level of this assembly	0	0	0	0	0	1	0	0	04	SSTL 2.5 V
9	DDR SDRAM cycle time, CL = X -A75B	0	1	1	1	0	0	0	0	70	CL = 2.5*1
	-B75B	0	1	1	1	0	1	0	1	75	
	-10B	1	0	0	0	0	0	0	0	80	
10	SDRAM access from clock (t_{AC}) -A75B/B75B	0	1	1	1	0	0	0	0	70	0.7 ns*1
	-10B	1	0	0	0	0	0	0	0	80	0.8 ns*1
11	DIMM configuration type	0	0	0	0	0	0	1	0	02	ECC
12	Refresh rate/type	1	0	0	0	0	0	1	0	82	7.8 µs Self refresh
13	Primary SDRAM width	0	0	0	0	0	1	0	0	04	× 4
14	Error checking SDRAM width	0	0	0	0	0	1	0	0	04	× 4
15	SDRAM device attributes: Minimum clock delay back-to-back column access	0	0	0	0	0	0	0	1	01	1 CLK
16	SDRAM device attributes: Burst length supported	0	0	0	0	1	1	1	0	0E	2, 4, 8
17	SDRAM device attributes: Number of banks on SDRAM device	0	0	0	0	0	1	0	0	04	4

Row/Col address bits

DQ/DQS buffer strength

CAS latency slowest

Refresh rate

Dmi control

Platform Conference

Chipset DRAM Timing Register Setup(2)

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
18	SDRAM device attributes: $\overline{CAS}$ latency	0	0	0	0	1	1	0	0	0C	2/2.5
19	SDRAM device attributes: $\overline{CS}$ latency	0	0	0	0	0	0	0	1	01	0
20	SDRAM device attributes: $\overline{WE}$ latency	0	0	0	0	0	0	1	0	02	1
21	SDRAM module attributes	0	0	1	0	0	1	1	0	26	Registered
22	SDRAM device attributes: General	0	0	0	0	0	0	0	0	00	± 0.2 V
23	Minimum clock cycle time at CLX - 0.5	0	1	1	1	0	1	0	1	75	CL = 2*[6]
	-A75B										
	-B75B/10B	1	0	1	0	0	0	0	0	A0	
24	Maximum data access time (t_{AC}) from clock at CLX - 0.5	0	1	1	1	0	0	0	0	70	0.7 ns*[5]
	-A75B/B75B										
	-10B	1	0	0	0	0	0	0	0	80	0.8 ns*[5]
25	Minimum clock cycle time at CLX - 1	0	0	0	0	0	0	0	0	00	
26	Maximum data access time (t_{AC}) from clock at CLX - 1	0	0	0	0	0	0	0	0	00	
27	Minimum row precharge time (t_{RP})	0	1	0	1	0	0	0	0	50	20 ns
28	Minimum row active to row active delay (t_{RRD})	0	0	1	1	1	1	0	0	3C	15 ns
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD})	0	1	0	1	0	0	0	0	50	20 ns
30	Minimum active to precharge time (t_{RAS})	0	0	1	0	1	1	0	1	2D	45 ns
	-A75B/B75B										
	-10B	0	0	1	1	0	0	1	0	32	50 ns
31	Module bank density	1	0	0	0	0	0	0	0	80	2 bank 512MB

Supported CAS latency

Registered DiMM

CAS latency 2nd slowest

CAS latency 3rd slowest
(Not supported in this case)

tRPmin

tRASmin

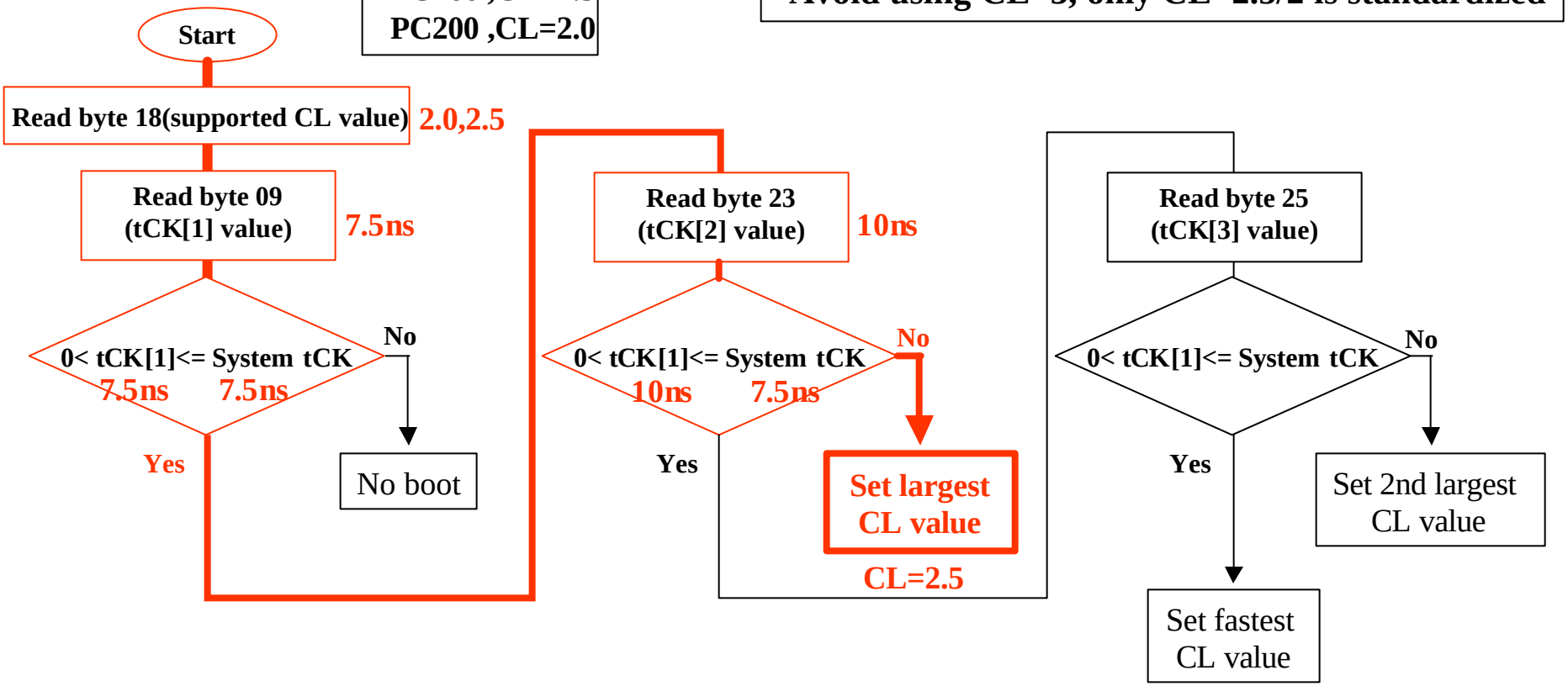
Setting up CL from SPD

@PC266 system

DiMM SPD

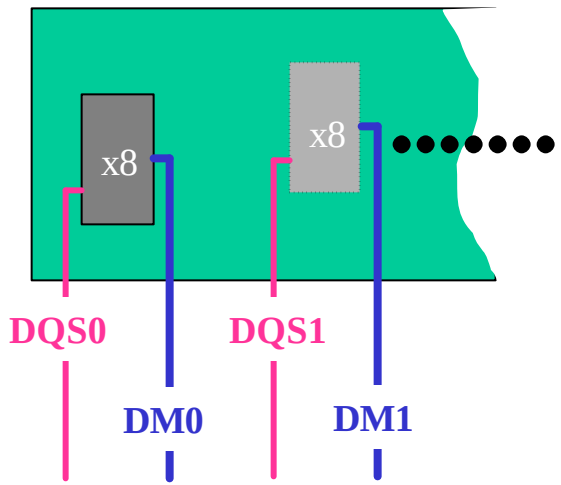
PC266 ,CL=2.5
PC200 ,CL=2.0

-Use SPD data
-Avoid using CL=3, only CL=2.5/2 is standardized

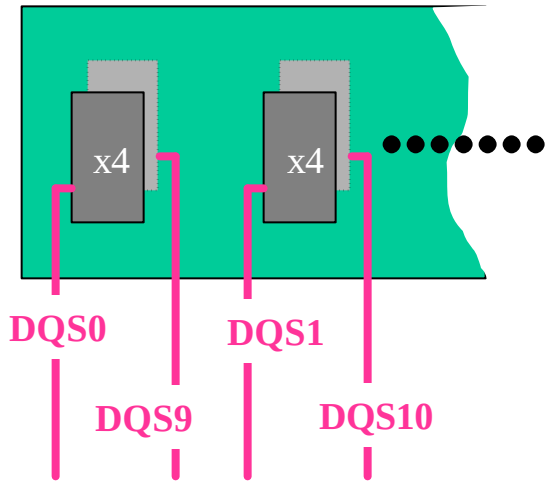


Dmi Signal routing

DIMM(x8 component)



DIMM(x4 component)



Dmi signal routing/driver needs to be the same as DQSi if system supports both x4 and x8 components.

Registered DiMM

- RESET pin is now open

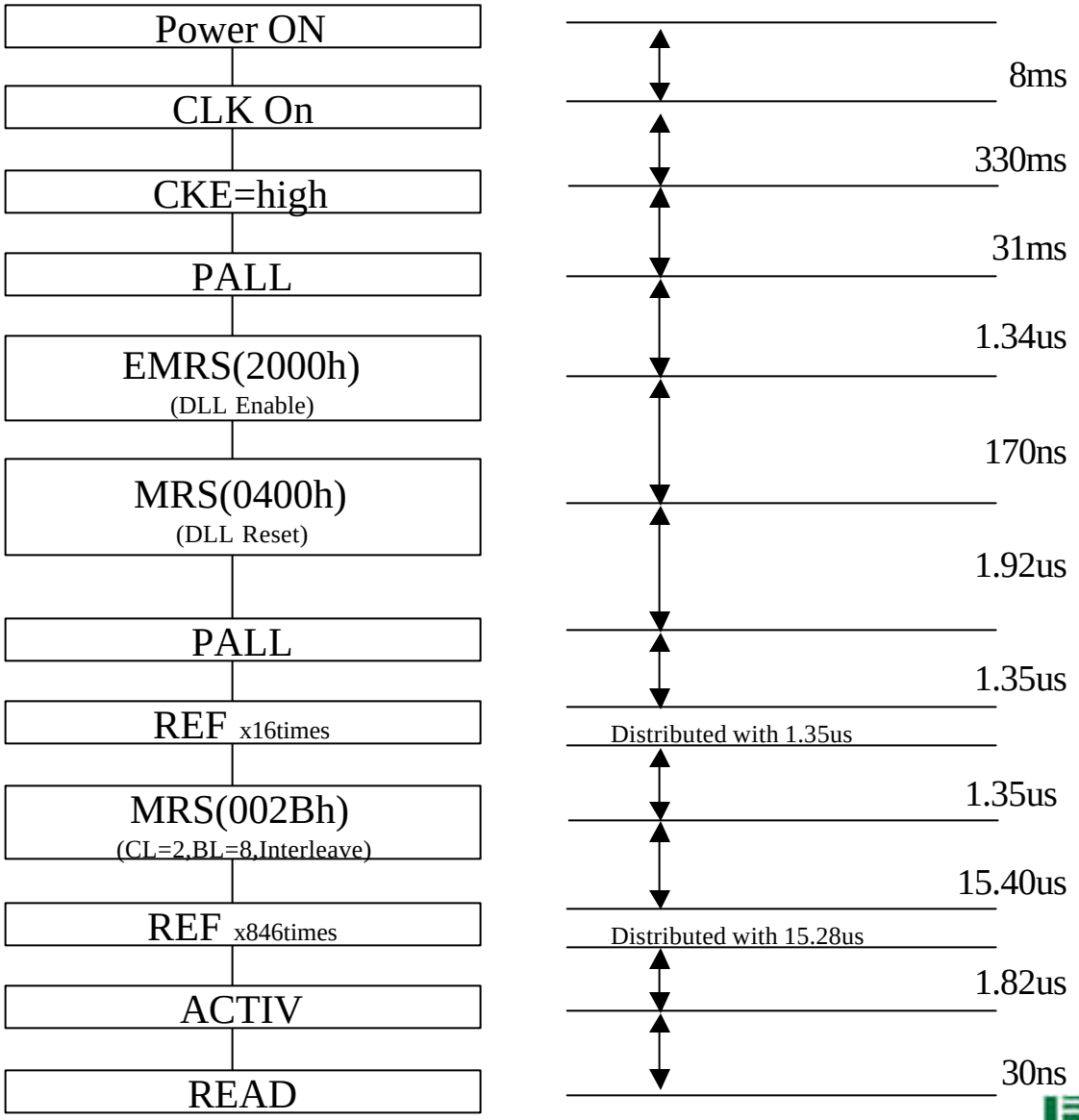
	184pin DiMM	168pin DiMM
RESET(pin10)	Open	Pull UP

Evaluation

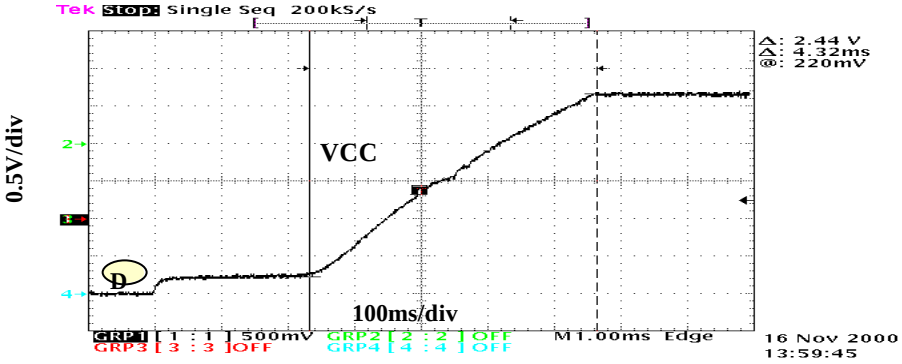
Major Evaluation items

- Power up sequence
- Noise
  - Signal Integrity
    - SSN
    - Cross Talk
    - Refrection
  - Vref, Vcc Noise
- Timing
  - CLK&/CLK jitter
  - Setup/Hold
- System Level Margin

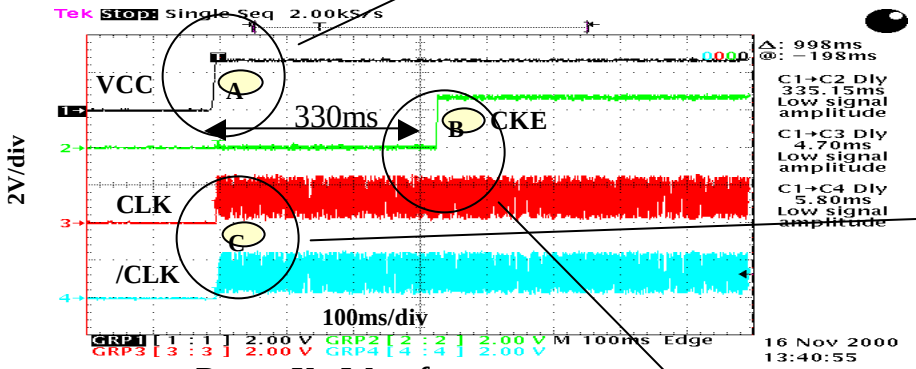
Power-up Sequence(measured)



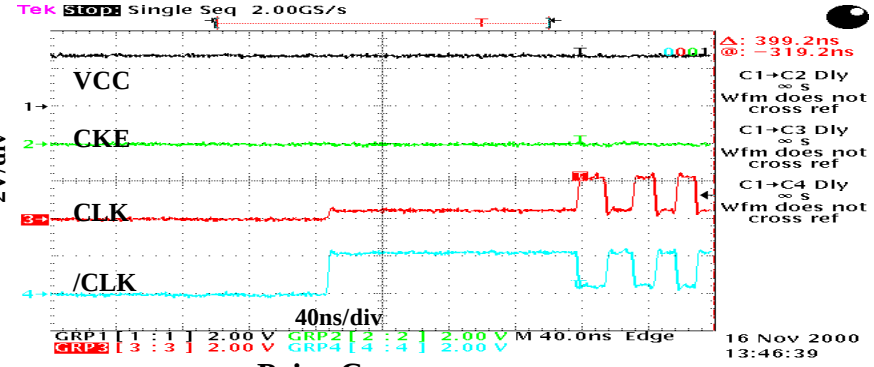
VCC,CLK,/CLK,CKE waveforms @power-up



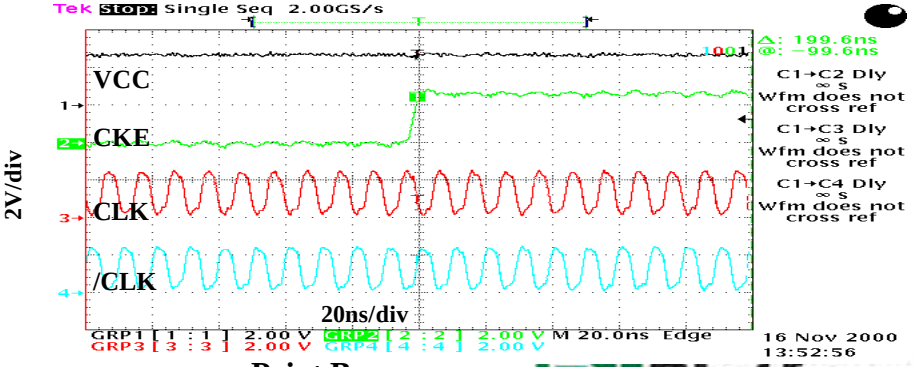
point A



Power Up Waveform



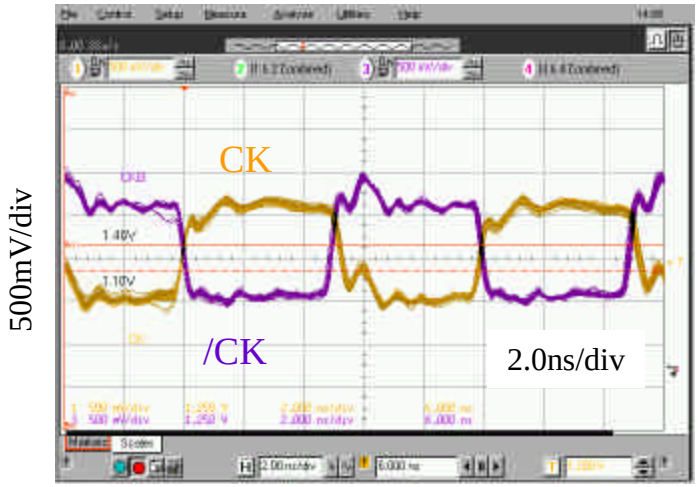
Point C



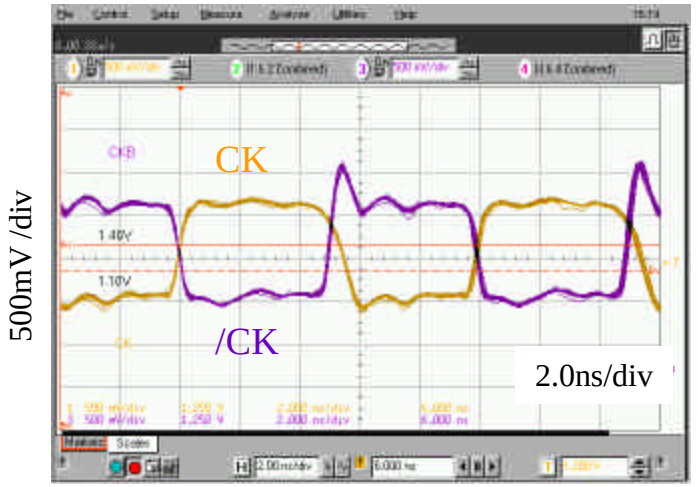
Point B

Waveforms @ different points

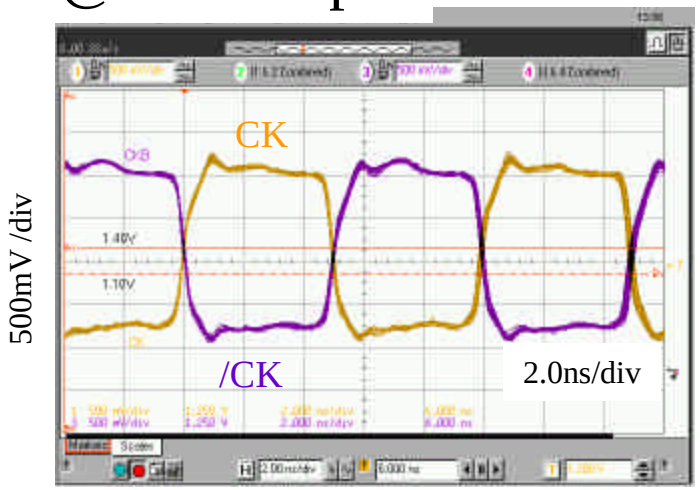
@Socket-pin



@PLL-via



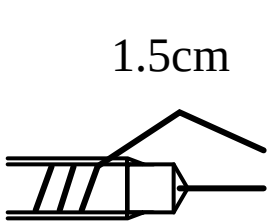
@DRAM-pin

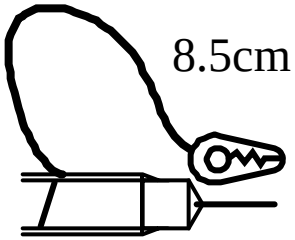


Make measurements at receiver pin

0.5GB Registered DIMM

Effect of GND wire(1)

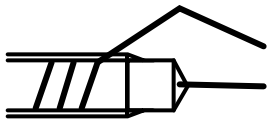




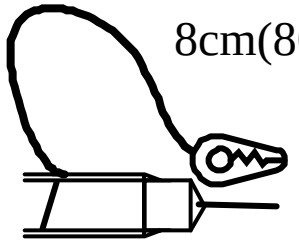
Long GND wire looses high frequency component.

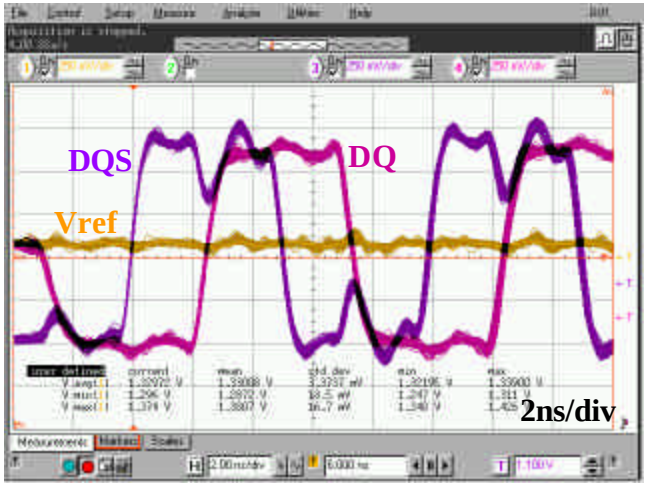
Effect of GND wire(2)

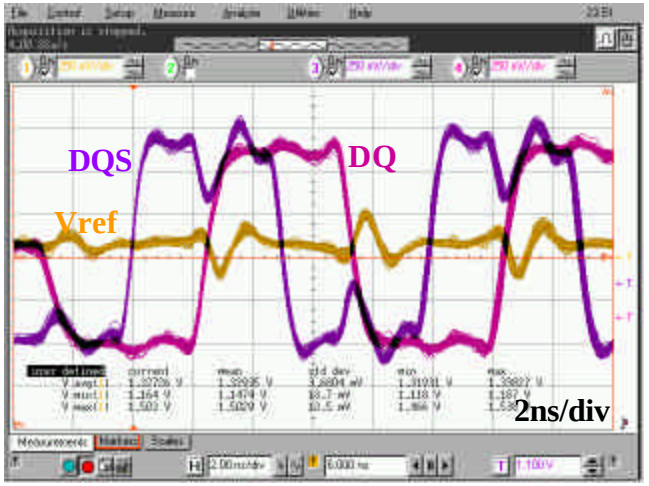
1.5cm(3.5mm2)



8cm(80mm2)







Long GND wire pickups realistic but unwanted noise.

Data Window Evaluation

4.16ns(@1.40V)
4.32ns(@1.30V)
4.16ns(@1.10V)

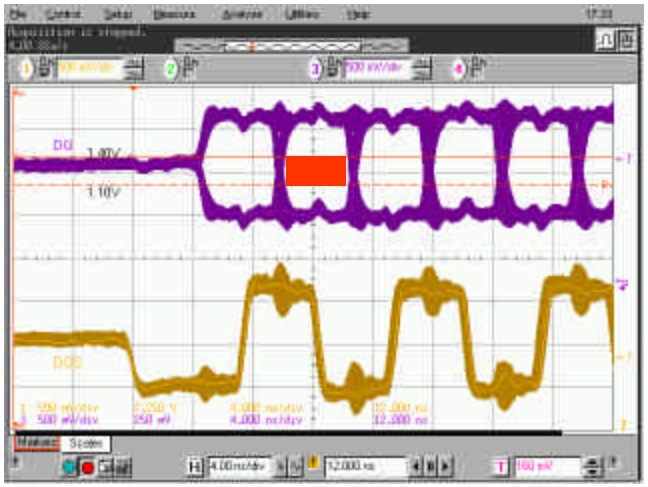


Fig.1 Slot1(0.5GBDIMM),Slot2(Empty)

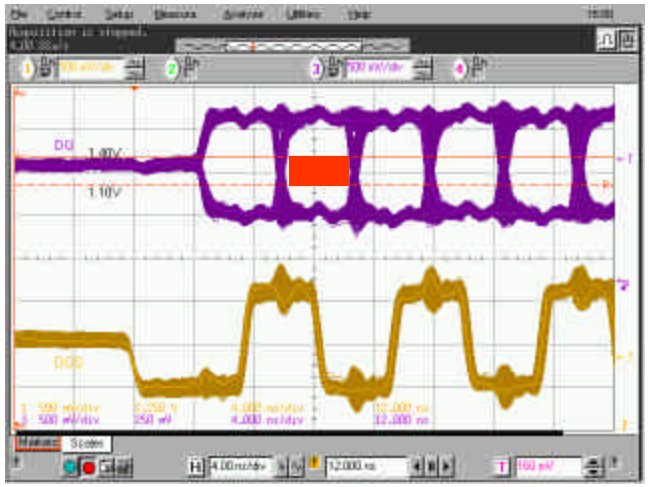


Fig.2 Slot1(Empty),Slot2(0.5GBDIMM)

4.00ns(@1.40V)
4.16ns(@1.30V)
4.08ns(@1.10V)

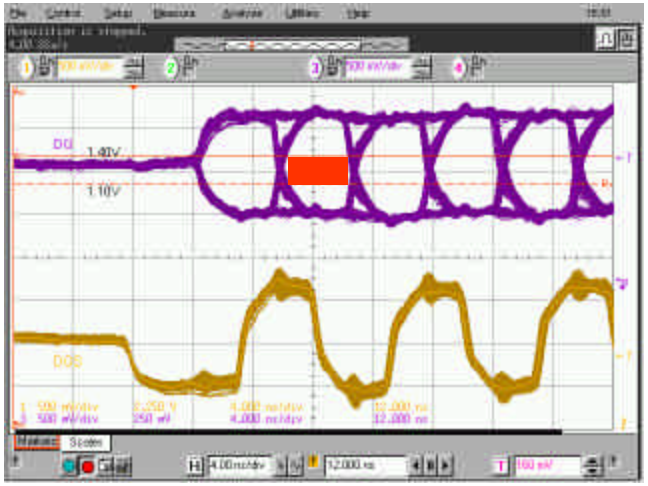


Fig.3 Slot1(1GBDIMM),Slot2(0.5GBDIMM)

3.92ns(@1.40V)
4.32ns(@1.30V)
3.84ns(@1.10V)

Data window needs more than 2.6ns for DDR1 system.

Vref Margin Test

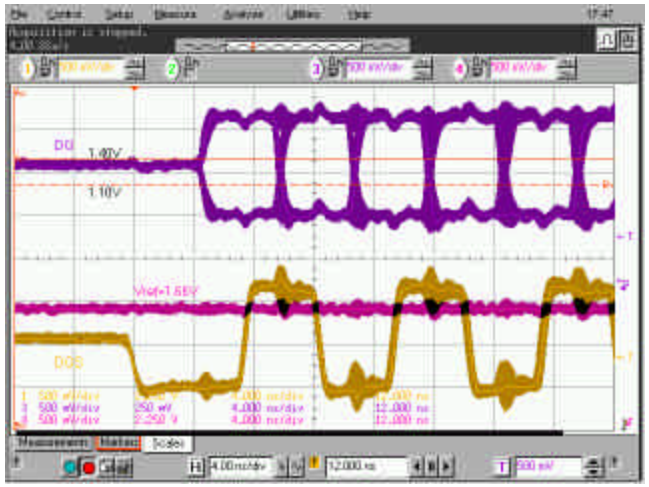


Fig.1 Vref=High(1.66V>1.52V)

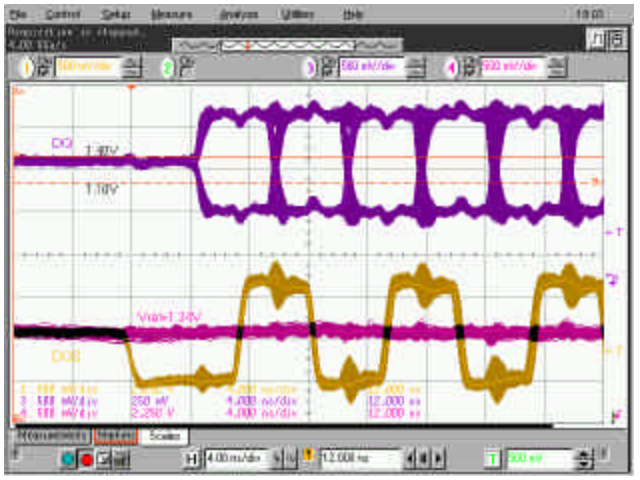


Fig.2 Vref=Center(1.34V)

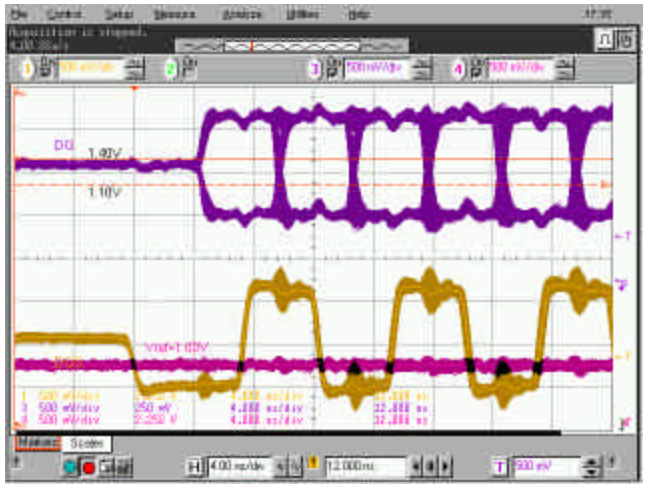


Fig.3 Vref=Low(1.00V<1.16V)

Vref margin needs more than +-0.18V for DDR1 system.

SSN Measurements Results(*PC200 Light load)*

- Very Important to control test pattern
- Memory Driver DQ power supply pin needs good decoupling caps to avoid spec violation on DQS pin.

[ns]

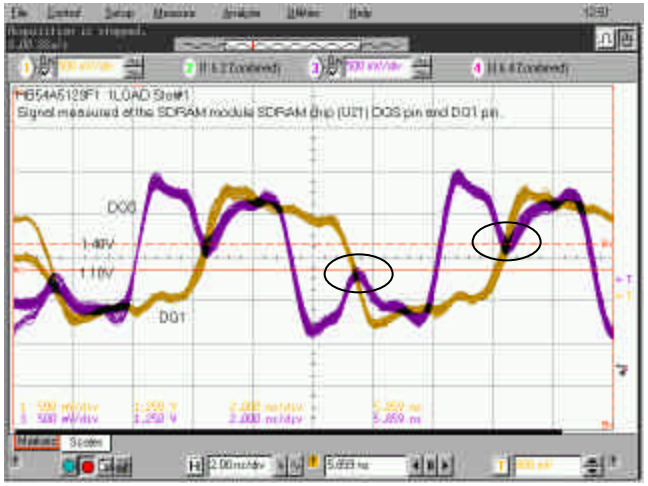


Fig.1-1 Pattern 0F0F

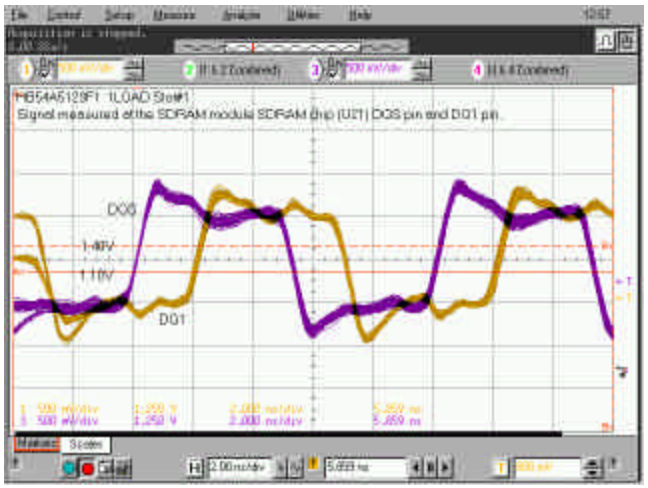


Fig.1-2 Pattern 5A5A

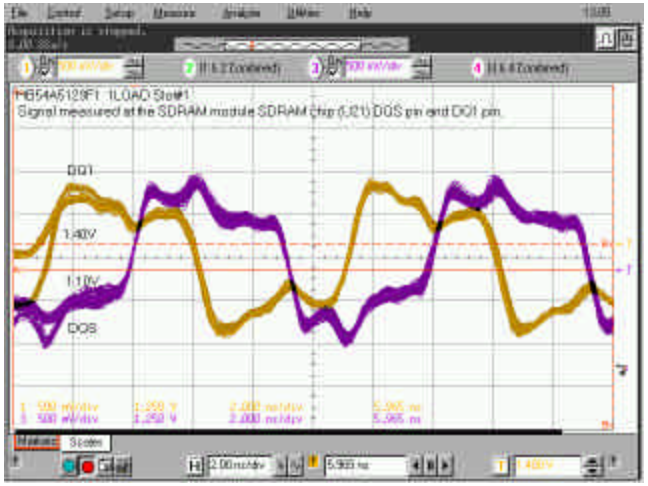


Fig.1-3 Pattern F0F0

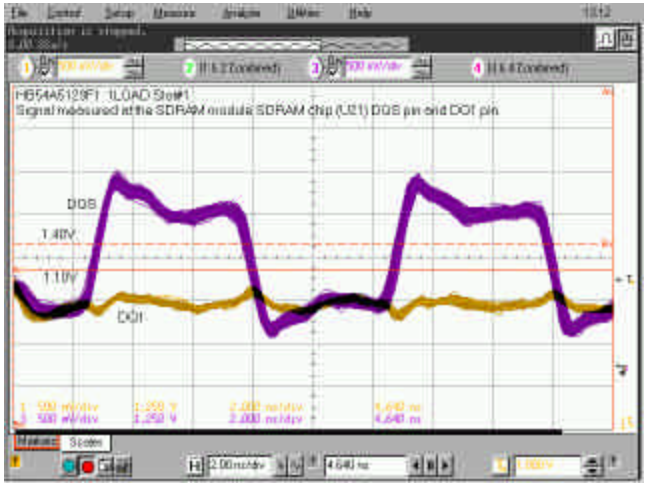
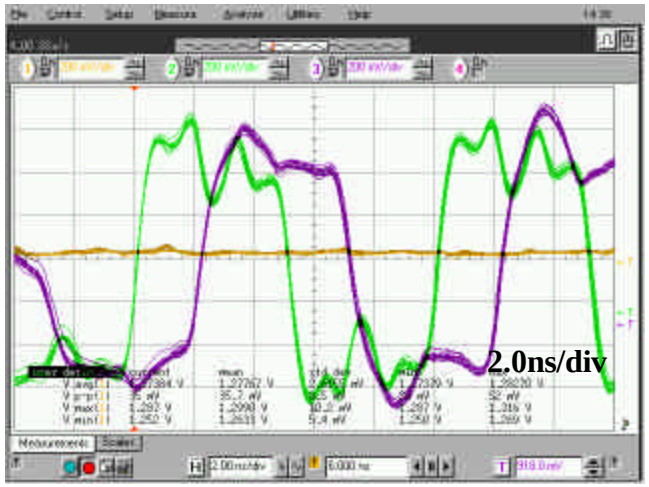


Fig.1-4 Pattern ALL0

Vref Noise Measurements Results(*PC200)*

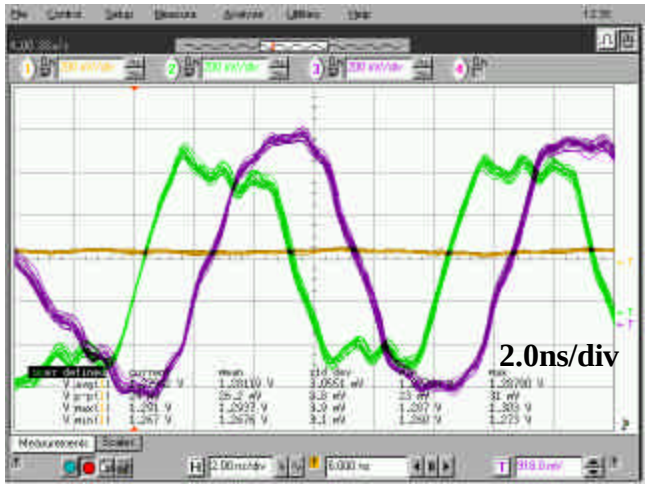
Vref noise should be within +-0.1V for DDR1 system for Write cycle.

Min.



Vref max. =1.316V
Vref min. =1.250V
Vref p-p =66mV

Full



Vref max. =1.303V
Vref min. =1.260V
Vref p-p =43mV

ELPIDA

Timing Evaluation

Platform Conference

Clock(*PC200)*

Table 1-14 Clock (@Socket pin) [ns]

	Min.	Max.	Mean.	Spec.	Margin	Notes	Fig.#
tCK	9.92	10.09	10.02	10.00	-	Clock Cycle time	Fig.1-34
tCH	4.99	5.15	5.08	4.5-5.5	0.35	Clock high level time	
tCL	4.86	5.02	4.93	4.5-5.5	0.36	Clock low level time	

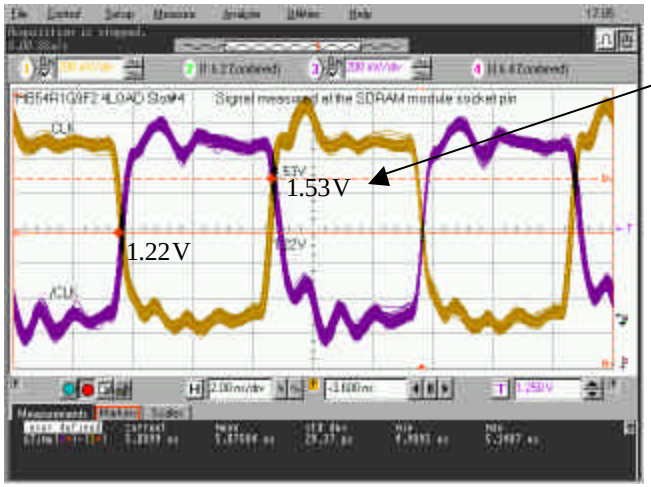
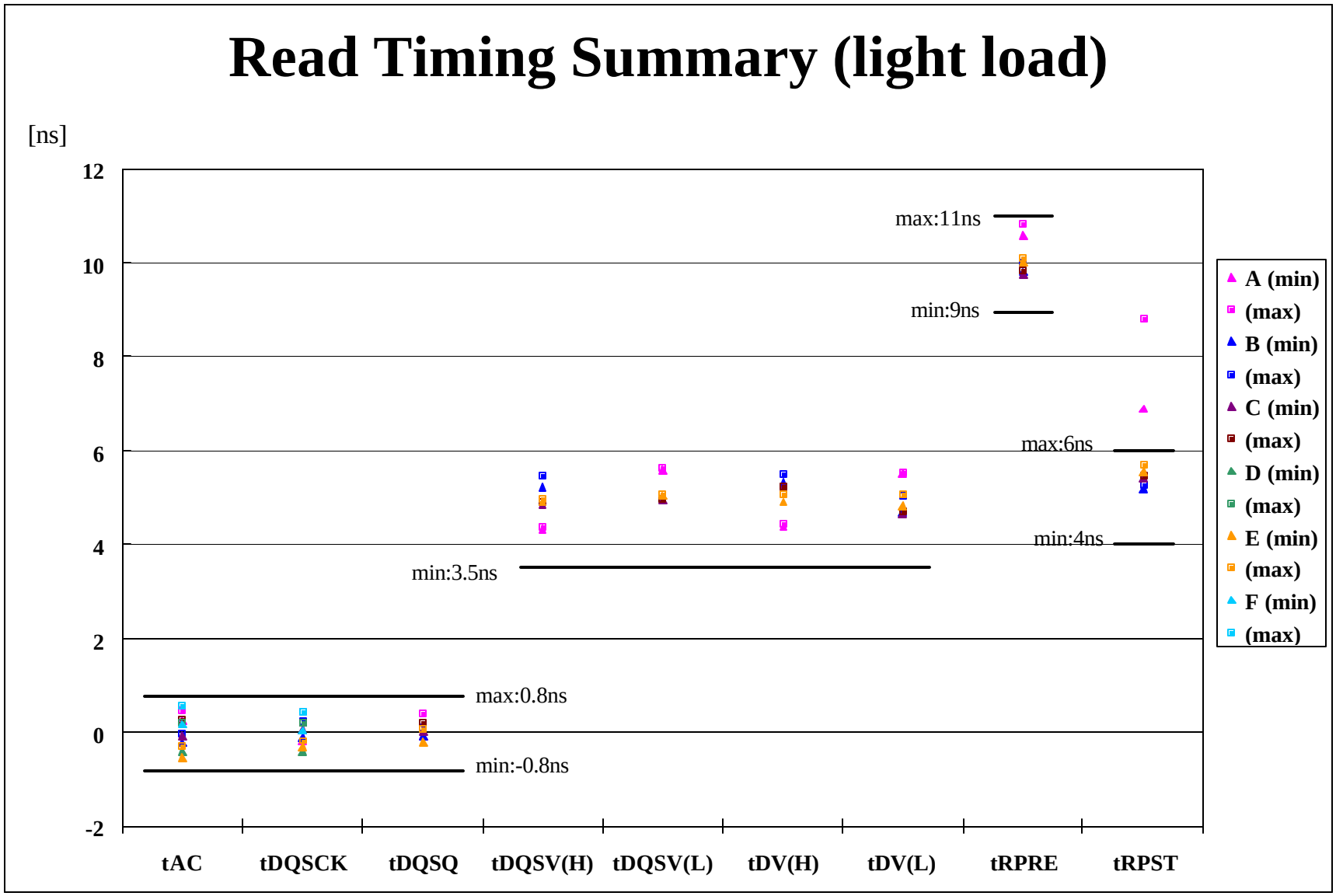


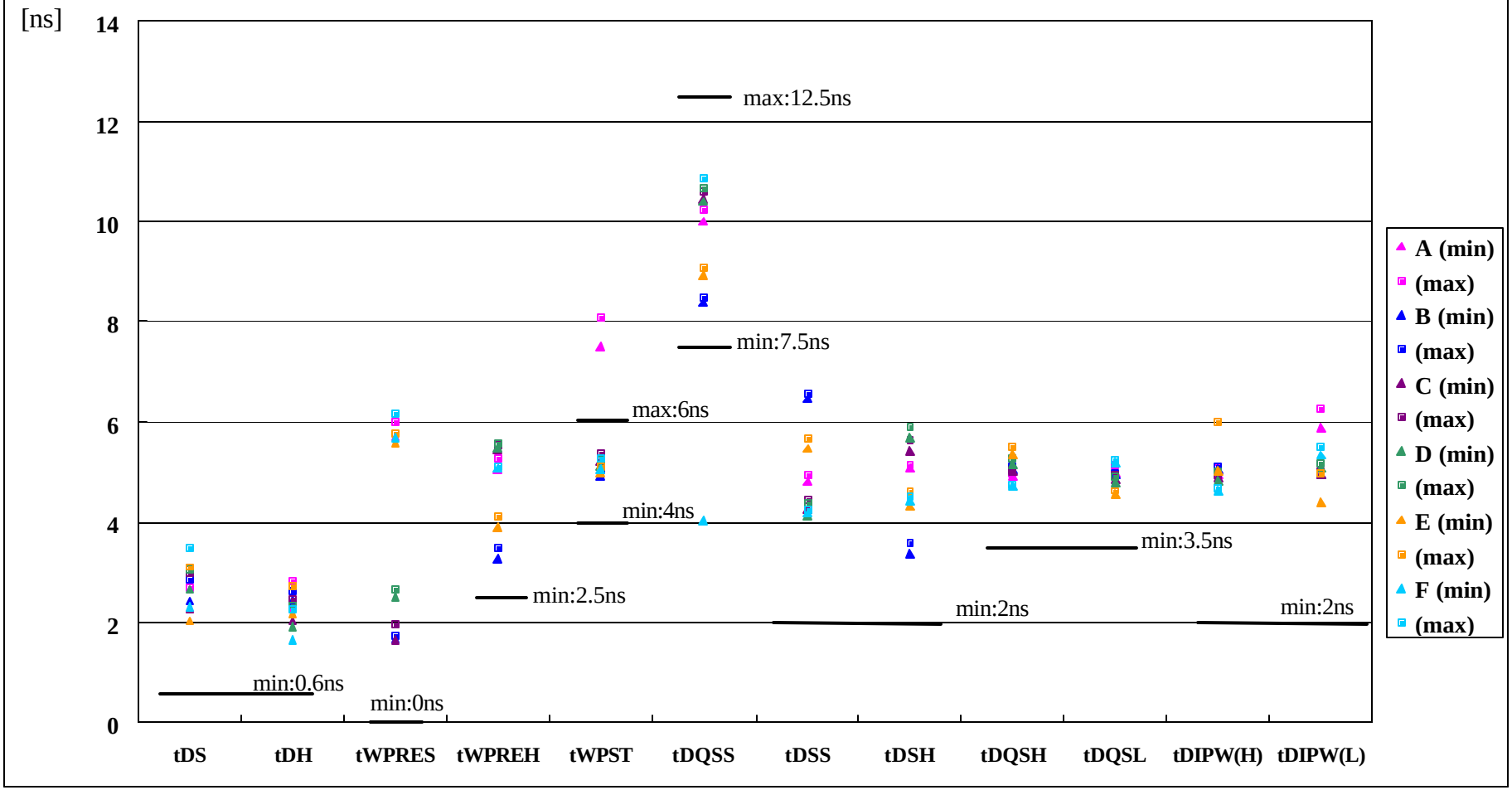
Fig.1-34

Recommends to have differential cross point at Vref+-0.2V to reduce timing jitter.

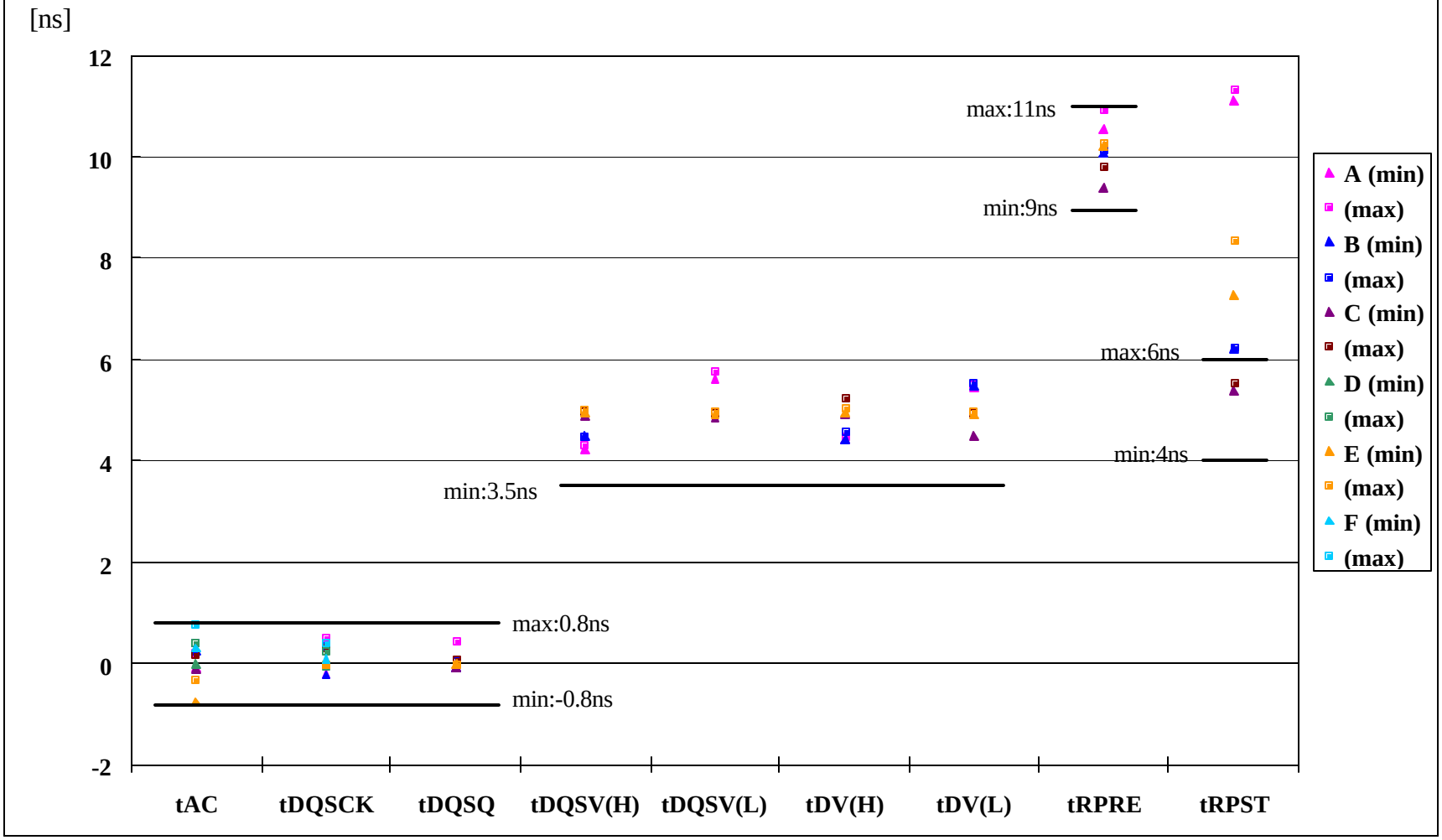
Read Timing Summary (light load)



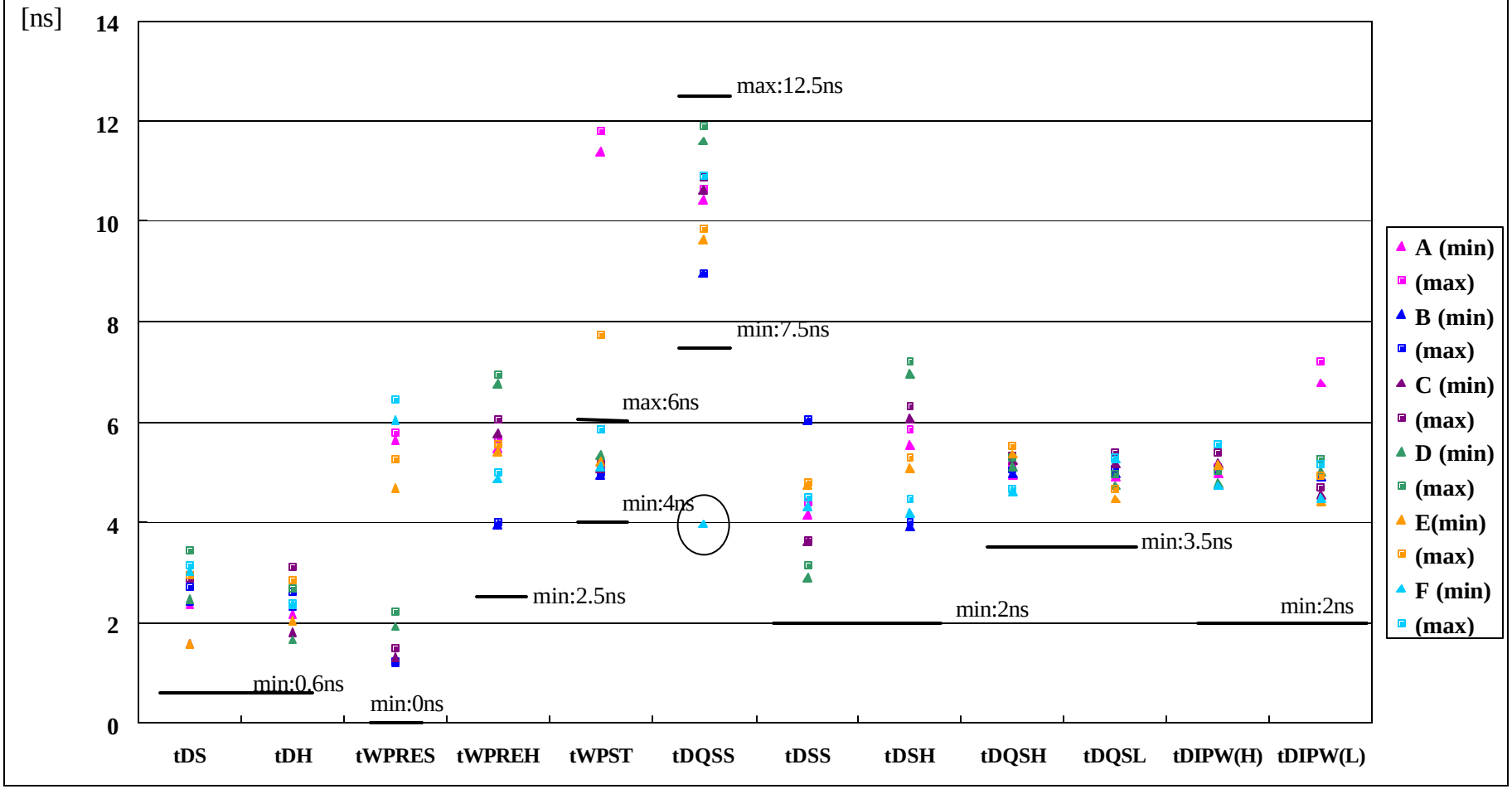
Write Timing Summary (light load)



Read Timing Summary (full load)



Write Timing Summary (full load)



CLK and ADD setup hold(*PC200 Full load)*

Table 1-4 CLK and ADD(A8) setup hold (@Socket pin)

[ns]

	Min.	Max.	Mean	Spec.	Margin	Notes	Fig.#
tIH	2.94	3.18	3.05	1.10	1.84	tAH falling	Fig.1-9
tIH	2.84	3.00	2.97	1.10	1.74	tAH rising	Fig.1-10
tIS	6.82	6.99	6.90	1.10	5.72	tAS falling	Fig.1-11
tIS	7.01	7.15	7.09	1.10	5.91	tAS rising	Fig.1-12

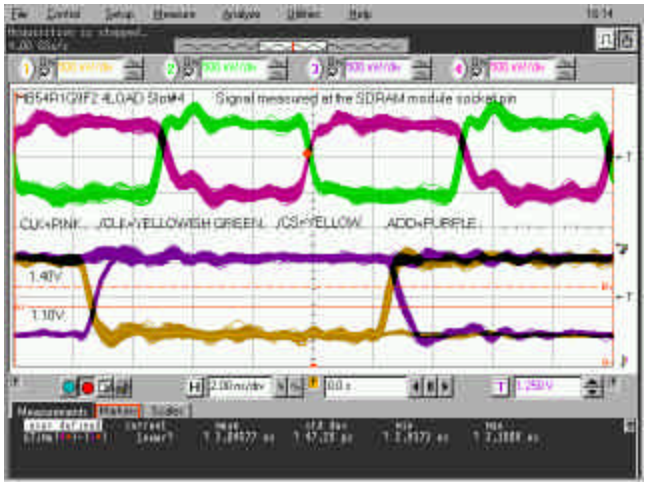


Fig.1-9

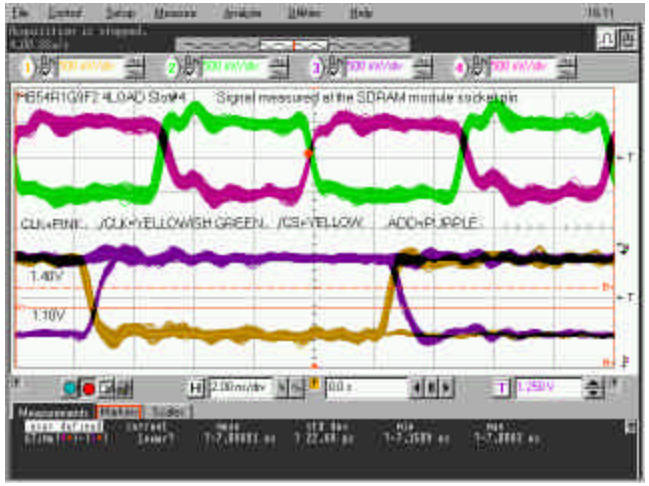


Fig.1-12

CLK and /CS setup hold(*PC200 Full load)*

Table 1-5 CLK and /CS setup hold (@Socket pin)

[ns]

	Min.	Max.	Mean	Spec.	Margin	Notes	Fig.#
tIH	2.53	2.67	2.60	1.10	1.43	tCH rising	Fig.1-13
tIS	7.25	7.37	7.32	1.10	6.15	tCS falling	Fig.1-14

Fig.1-13

Fig.1-14

Write DQ/DQS setup hold(*PC200 Full load)*

Table 1-10 Write DQ/DQS setup hold (@DRAM)

[ns]

	Min.	Max.	Mean	Spec.	Margin	Notes	Fig.#
tDH	1.66	2.17	1.90	0.60	1.06	DQ falling edge Hold time against DQS falling edge	
tDH	1.95	2.40	2.17	0.60	1.35	DQ falling edge Hold time against DQS rising edge	
tDH	1.96	2.67	2.19	0.60	1.36	DQ rising edge Hold time against DQS falling edge	
tDH	1.84	2.36	2.10	0.60	1.24	DQ rising edge Hold time against DQS rising edge	Fig.1-29
tDS	2.59	3.15	2.97	0.60	1.99	DQ falling edge against DQS falling edge setup time	Fig.1-30
tDS	2.72	3.34	3.01	0.60	2.12	DQ falling edge against DQS rising edge setup time	
tDS	2.75	3.44	3.04	0.60	2.15	DQ rising edge against DQS falling edge setup time	
tDS	2.48	3.01	2.76	0.60	1.88	DQ rising edge against DQS rising edge setup time	

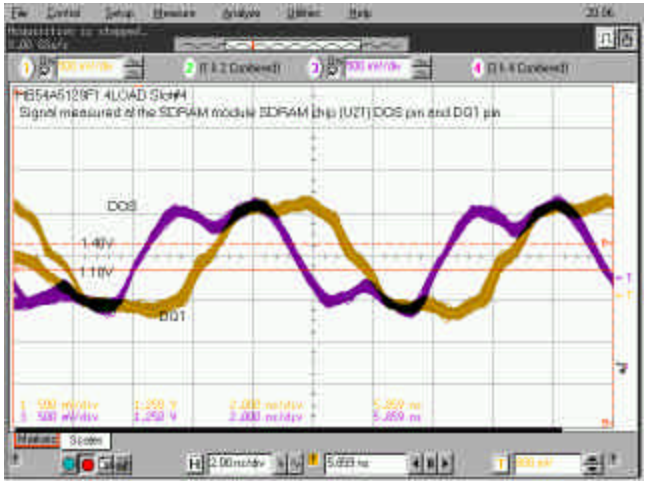


Fig.1-29

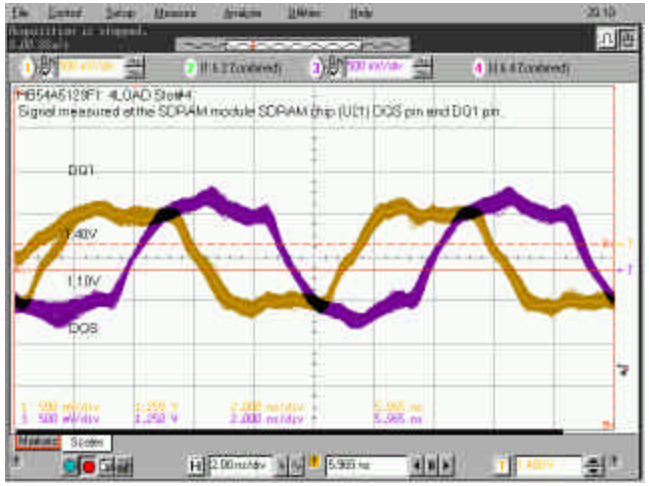


Fig.1-30

Write DQ/DQS setup hold(*PC200 Light load)*

Table 2-10 Write DQ/DQS setup hold (@DRAM)

	Min.	Max.	Mean	Spec.	Margin	Notes	Fig.#
tDH	2.07	2.31	2.18	0.60	1.57	DQ2 rising edge Hold time against DQS0 rising edge	
tDH	2.14	2.33	2.23	0.60	1.64	DQ2 falling edge Hold time against DQS0 rising edge	
tDH	1.92	2.06	2.00	0.60	1.42	DQ2 falling edge Hold time against DQS0 falling edge	
tDH	2.05	2.16	2.11	0.60	1.55	DQ2 rising edge Hold time against DQS0 falling edge	Fig.2-22
tDS	2.65	2.81	2.73	0.60	2.15	DQ2 rising edge against DQS0 rising edge setup time	Fig.2-23
tDS	2.85	2.91	2.91	0.60	2.35	DQ2 falling edge against DQS0 rising edge setup time	
tDS	2.81	3.06	2.96	0.60	2.31	DQ2 rising edge against DQS0 falling edge setup time	
tDS	2.84	3.02	2.95	0.60	2.34	DQ2 falling edge against DQS0 falling edge setup time	

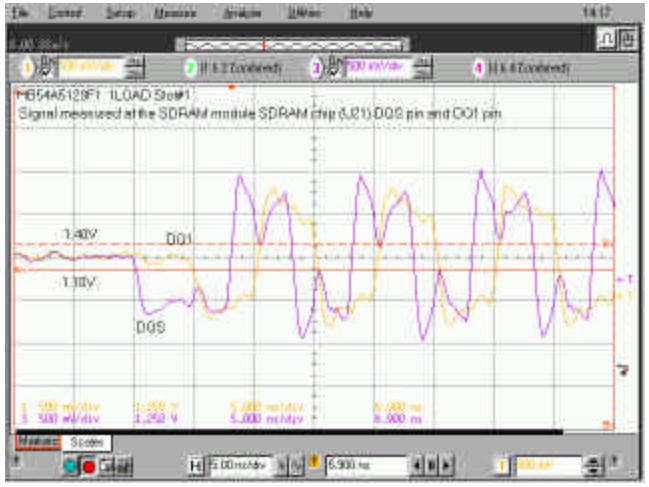


Fig.2-22

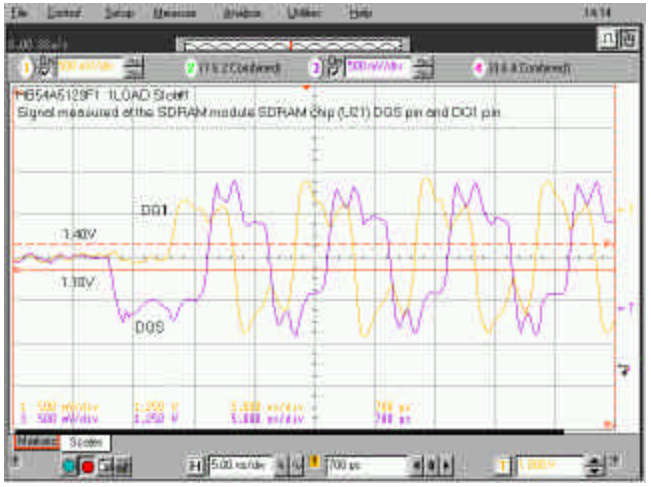


Fig.2-23

Sequence Timing Measurements Results(*PC200)*

Timing Measurement

Item.	Spec.[x tCK(10ns)]		Measured value[x10ns]	
	min.	max.	min.	max.
CL	2/2.5/3		2	
BL	1/2/4/8/Full Page		8	
tRCD	2	-	2	14
tRP	2	-	2	1600
tRAS	5	12000	6(READ), 9(WRITE)	4622
tRC	7	-	8(READ), 11(WRITE)	4625
tWR	2	-	2	4570
tRRD	2	-	2	8

CKE is Always H.
DM is Always L.
Auto Precharge mode is not used.

Refresh

Item.	Spec.		Measured value	
	min.	max.	min.	max.
tREF	64ms		126ms	
REF Command distribution	7.6us(average)	-	90ns	46.25us

This system tREF value is 126ms(15.3us/row), but specification of tREF is 64ms(7.8us/row).
Please review the refresh rate setting.

Memory Operation Modes State

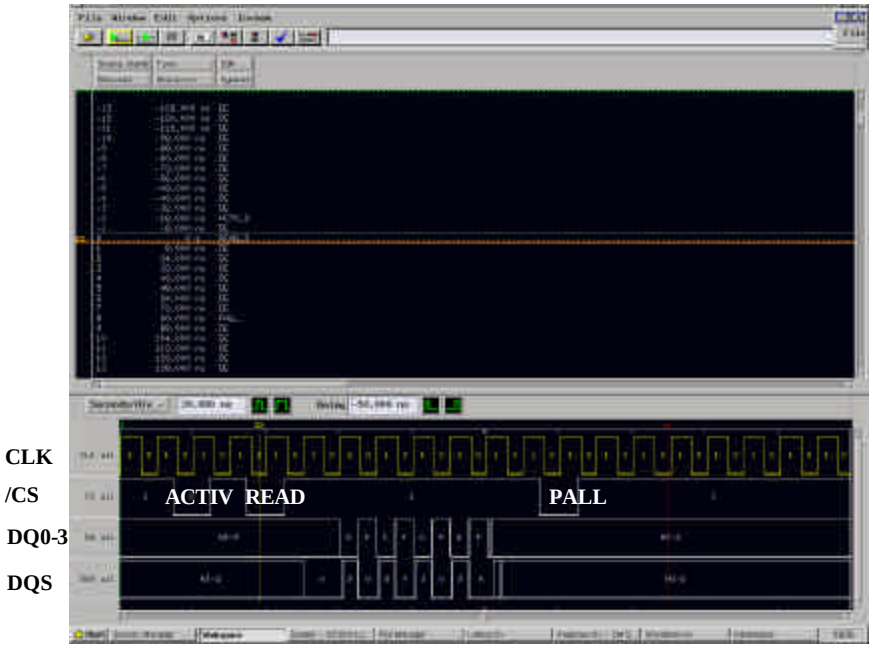


Fig.1 ACTIV-READ-PALL

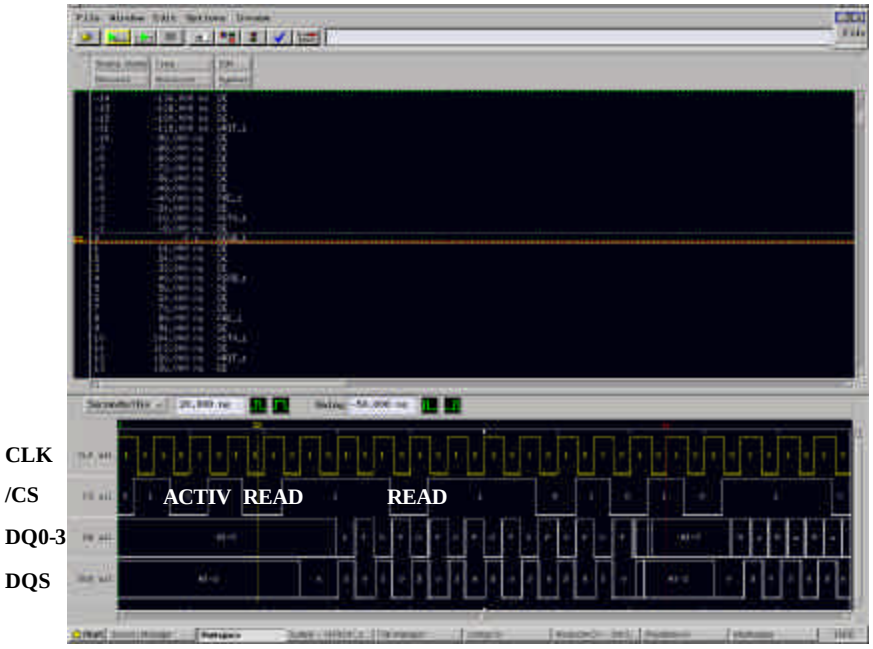
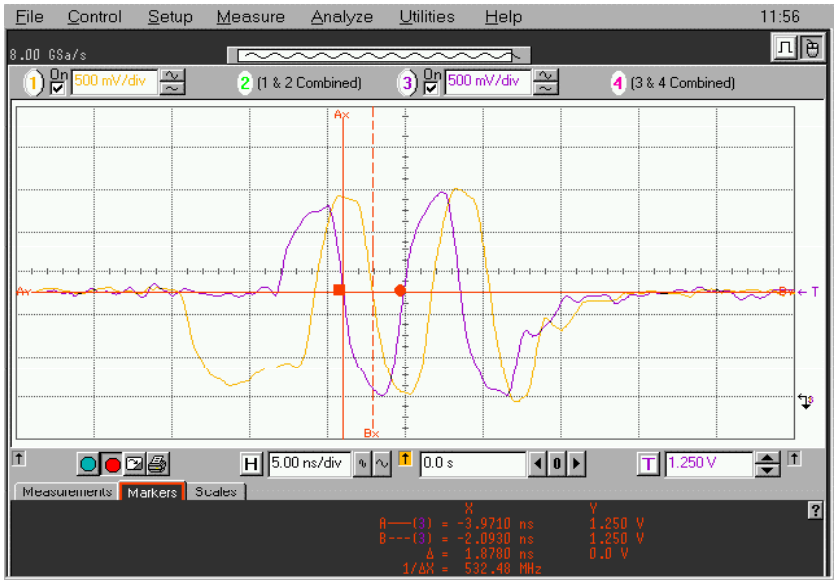
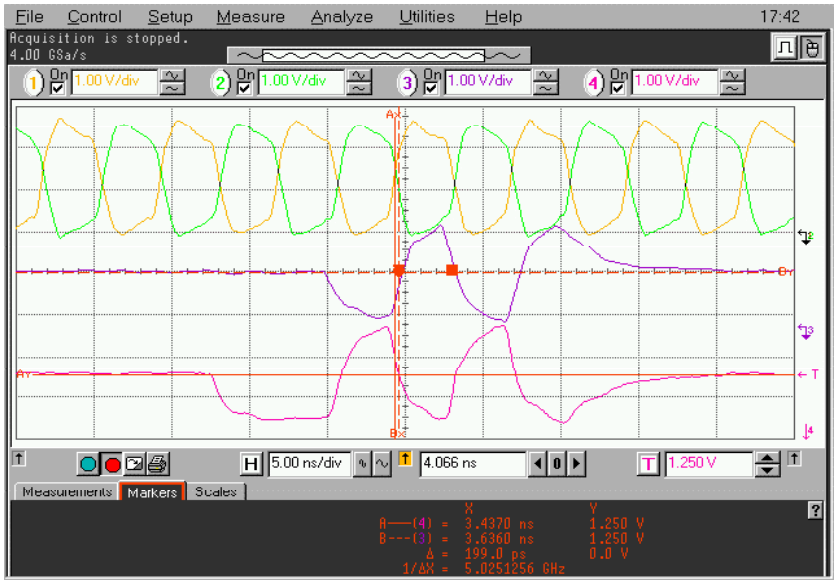


Fig.2 ACTIV-READ-READ <Consecutive Burst>

4GB DDR System in operation @ 266Mbps

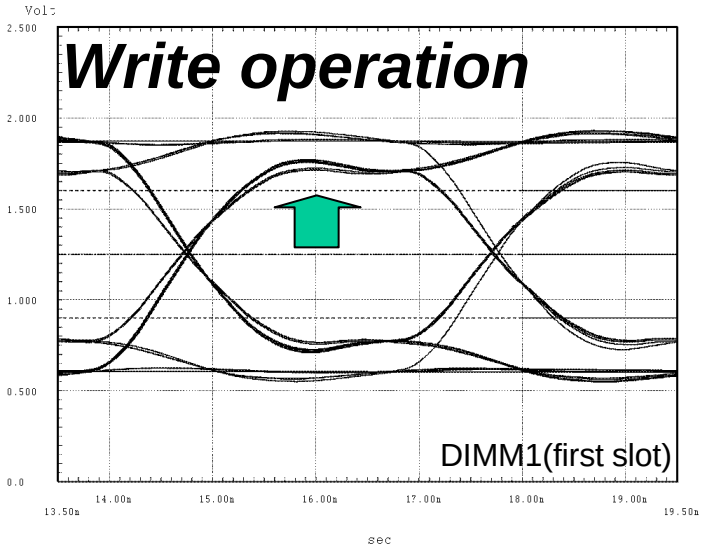


Write DQ & DQS @ DRAM

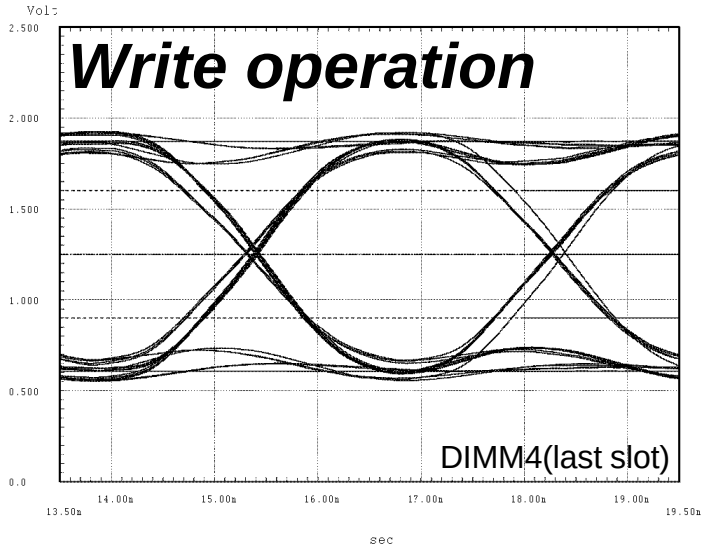


Read CLK DQ & DQS @ Chipset

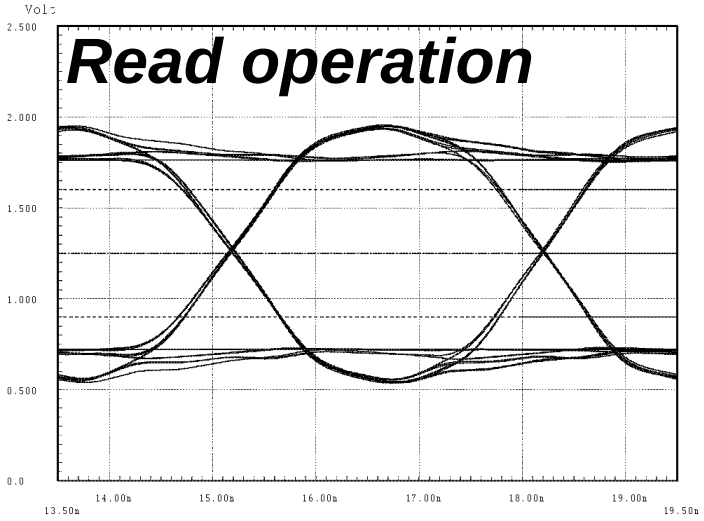
DDR333 2bank 4slot



Eyepattern @DRAM receiver



Eyepattern @DRAM receiver



Eyepattern @Controller receiver

2Bank_4slot

Short stub

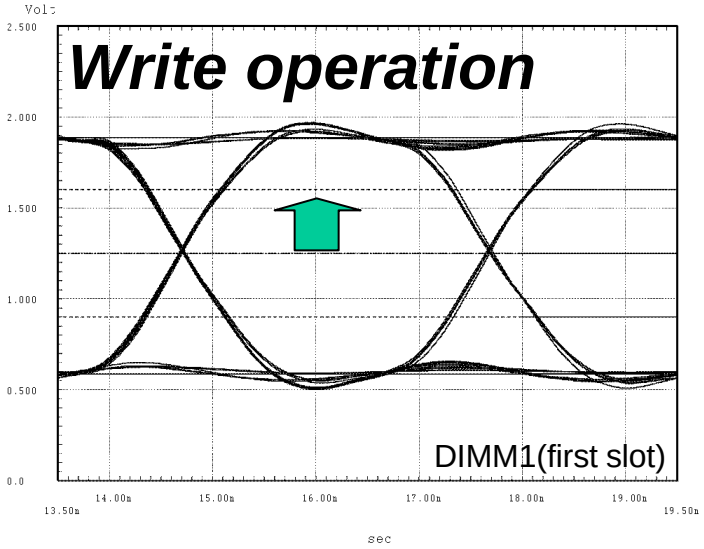
TSOP

Condition: typical

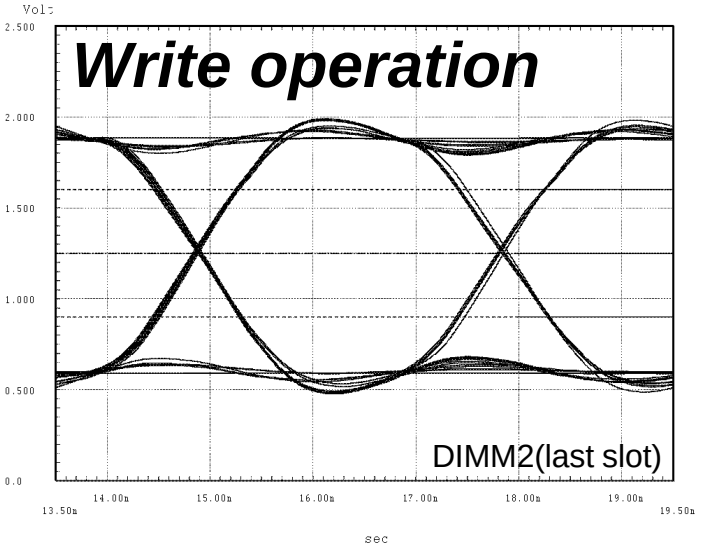
Device typ. Vddq=2.5V, Tj=27C

Platform Conference

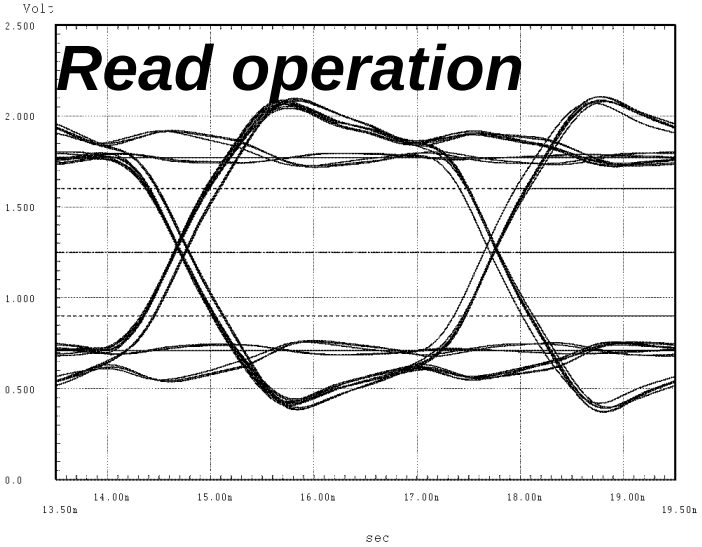
DDR333 2bank 2slot



Eyepattern @DRAM receiver



Eyepattern @DRAM receiver



Eyepattern @Controller receiver

2Bank_2slot

TSOP

Condition: typical
Device typ. Vddq=2.5V, Tj=27C